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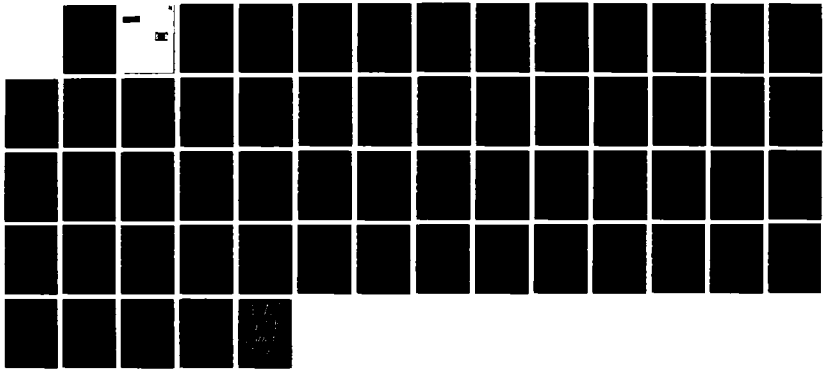

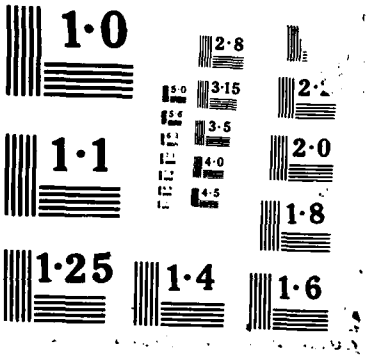
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SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No 0704-0188
Exp Date Jun 30 1986

1a REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b DECLASSIFICATION/DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S) HDL-TR-2137	5 MONITORING ORGANIZATION REPORT NUMBER(S)
6a NAME OF PERFORMING ORGANIZATION Harry Diamond Laboratories 6b OFFICE SYMBOL (If applicable) SLCHD-NW-RC	7a NAME OF MONITORING ORGANIZATION
6c ADDRESS (City, State, and ZIP Code) 2800 Powder Mill Road Adelphi, MD 20783-1197	7b ADDRESS (City, State, and ZIP Code)
8a NAME OF FUNDING/SPONSORING ORGANIZATION Defense Nuclear Agency 8b OFFICE SYMBOL (If applicable)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c ADDRESS (City, State, and ZIP Code) Washington, DC 20301	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. 6.2120.H; PROJECT NO.; TASK NO.; WORK UNIT ACCESSION NO 00213

11 TITLE (Include Security Classification)
Development of the Field-Induced Electron Injection and Impact Ionization (F4I) Technique for Radiation Hardness Testing of MOS Gate Insulators

12 PERSONAL AUTHOR(S)
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13a TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
Final	FROM 1980 TO 1983	March 1988	62

16 SUPPLEMENTARY NOTATION
HDL project: 237823
This work was sponsored by the Defense Nuclear Agency as part of the Hardness Assurance Program.

17 COSATI CODES		
FIELD	GROUP	SUB-GROUP
09	01	
14	02	

18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
Hardness assurance, MOS, Fowler-Nordheim tunneling, impact ionization, hole trapping, interface traps, radiation effects

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

Results are presented of an effort to develop an all-electrical means for simulating the effects of ionizing radiation on the radiation-sensitive oxide layers of metal-oxide-semiconductor (MOS) microelectronic devices. The report describes the field-induced electron injection and impact ionization (F4I) technique, its successful demonstration, and successful correlation of F4I test results with conventional radiation hardness tests using an ionizing radiation source (^{60}Co). Also described are the development and operation of a microcomputer-controlled test system that permits semiautomatic application of the F4I test to circuit test structures.

20 DISTRIBUTION/AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL Harold E. Boesch	22b TELEPHONE (Include Area Code) (202) 394-3180 22c OFFICE SYMBOL SLCHD-NW-RC

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted
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FOREWORD

This document constitutes a final report on work performed by the Radiation Effects Physics Group at the Harry Diamond Laboratories (HDL) during FY 1980-1983 under both Army 6.1 and Defense Nuclear Agency 6.2 (TREE Hardness Assurance Program) sponsorship. The intent of the effort, as indicated in the body of the text, was to explore the possibility of developing a promising electrical technique (field-induced electron injection and impact ionization-F4I), as a means for easily and reliably characterizing the total-dose radiation hardness of metal-oxide-semiconductor (MOS) integrated circuits, in a test to be performed preferably at the wafer level, near a process line, and in a routine manner by technicians. This effort was successful--the F4I technique works, and a usable test system was developed. Nevertheless, the effort was overtaken by another--in particular, the development of a commercially available low-energy x-ray source specifically designed for on-wafer irradiation of integrated circuits. While some difficulties have been experienced with correlating results obtained with more standard, higher energy sources (e.g., ^{60}Co), an x-ray system has the advantages of (1) being a "real" ionizing radiation source; (2) allowing irradiation of complete circuits as well as test structures; and (3) being presently commercially available. In the face of these facts, development of the F4I test was deemphasized in late 1982. Despite discontinuation of formal development of an F4I test system at HDL, the F4I technique has since been successfully applied as a research tool at several laboratories and universities for examining the behavior of MOS devices, and at least one laboratory is continuing investigation of the technique as a radiation hardness assurance tool. For this reason this report was prepared.

CONTENTS

FIGURES

FIGURES (cont'd)

1. INTRODUCTION

Military electronic systems currently being fielded or under development employ integrated circuits (IC's) of increasing complexity. As IC complexity has advanced, the IC technologies which employ metal-oxide-semiconductor (MOS) field-effect transistors as the basic circuit elements have assumed a dominant position. These technologies include n-channel and p-channel MOS (NMOS and PMOS) and complementary MOS (CMOS), along with variants such as silicon-on-sapphire (SOS) MOS and silicon-on-insulator (SOI) MOS. The great bulk of commercial large-scale-integration (LSI) or very-large-scale-integration (VLSI) integrated circuits, including microprocessors, semiconductor memories, and peripherals, are constructed in one or more of these MOS technologies.

The major effect of ionizing radiation from a space or nuclear weapon environment on an MOS IC is generation of electron/hole pairs in the silicon dioxide (SiO_2) insulating layers of the device. These layers include the thin gate insulator between the gate electrode and active channel region in the Si in each MOS field-effect transistor (MOSFET) and the thicker field oxide insulator which surrounds and isolates most of the structures. Radiation damage in the gate oxide has received the greatest attention, since this directly affects the operating point and characteristics of the individual MOSFET's in a circuit. The primary ionizing radiation effect in the SiO_2 layers is generation of electron/hole pairs. In a typical device-quality thermally grown oxide, the radiation-generated electrons are rapidly (within picoseconds) swept out of the oxide by any electrical bias applied between the gate electrode and the Si substrate. The radiation-generated holes, on the other hand, move relatively slowly through the oxide and, under worst-case (gate-positive) bias, some fraction of them are trapped in the oxide near the SiO_2/Si interface. This trapped positive-charge distribution causes a negative shift in the operating point or threshold voltage (V_t) of the MOSFET. The radiation-generated holes can also cause production of interface states at the SiO_2/Si interface, causing additional changes in the operating point and gain of the MOSFET. If these changes become too severe, device failure may result.

The vulnerability of MOS devices to radiation damage has usually been determined by exposing test devices to ionizing radiation from a variety of high-energy radiation sources: ^{60}Co, flash x-ray machines, electron linear accelerators (Van de Graaf machines, LINAC's), and pulsed reactors. Testing procedures using such sources generally cannot be applied on or near the process line at the wafer level and are usually time-consuming and expensive. Lower energy ionizing-radiation sources such as scanning electron microscopes [1-3] and vacuum ultraviolet sources [4] have been used in radiation hardness testing but have not received wide acceptance. As discussed in the foreword, during the period of this effort (FY 1980-83), use of a 10-keV x-ray source for on-wafer testing was also proposed. One purely electrical means for investigating hole and electron trapping in SiO_2 is avalanche charge injection into the SiO_2 from the Si substrate [5,6]. Application of this technique to radiation hardness assurance is complicated by the need to employ negative bias and highly doped Si substrates for hole injection. In work published in

1979, we described another all-electrical technique for the simulation of radiation damage in MOS structures. This technique--field-induced electron injection and impact ionization (F4I) [7]--and means for applying it received a patent: U.S. Patent 4,323,842, issued April 6, 1982.

Sections 2 and 3 of this report review the physical principles behind the F4I test and the early experiments performed to verify and demonstrate the technique and its ability to simulate radiation damage in MOS structures. Section 4 describes an effort to assess and ameliorate the effect of dielectric breakdown on the applicability of the F4I test. Section 5 then describes the development and function of a prototype F4I test system, and section 6 presents representative test results obtained with this system.

2. REVIEW OF THEORETICAL BASIS FOR F4I TECHNIQUE

The active region of all MOS devices consists essentially of a parallel-plate capacitor with a metal or polysilicon gate electrode, a silicon substrate counterelectrode, and an intervening SiO_2 gate insulator dielectric. Energy band diagrams for this structure are shown schematically in figure 1. The F4I technique takes advantage of two processes which operate in an MOS structure when a very large positive field (gate positive with respect to substrate) is applied across the SiO_2 gate oxide (fig. 1b). The first process is Fowler-Nordheim tunneling of electrons into the oxide. The second process is creation of electron/hole pairs in the SiO_2 by interaction of field-accelerated electrons with the oxide via impact ionization. Once created, the electron/hole pairs are indistinguishable from those produced by ionizing radiation (fig. 1a): the electrons contribute slightly (typically ~1 percent) to the tunneling current through the oxide toward the gate electrode, while the holes transport toward the Si where they may escape into the Si or interact to become trapped or lead to interface-state production.

Fowler-Nordheim tunneling of electrons from the conduction band of the Si is strongly electric-field dependent and is described by the expression

$$J = AE^2 \exp(-B/E) \quad , \qquad (1)$$

where J is the electron current density, E is the applied field across the oxide (neglecting space charge), and A and B are constants for the material. The values of these constants were obtained from the work of previous investigators [8-10]: $A = 2 \times 10^6$ A/MV^2 and B = 238 MV/cm. (The determination of A is subject to large errors. The given value is a best estimate from several references and, for the stated value of B, is believed accurate within a factor of two.)

After being injected into the conduction band of the oxide, electrons drift under the influence of the electric field. At fields above ~8 MV/cm, a small fraction of the electrons acquire enough energy (~9 eV) between scattering events to produce electron/hole pairs in the oxide by impact ionization.

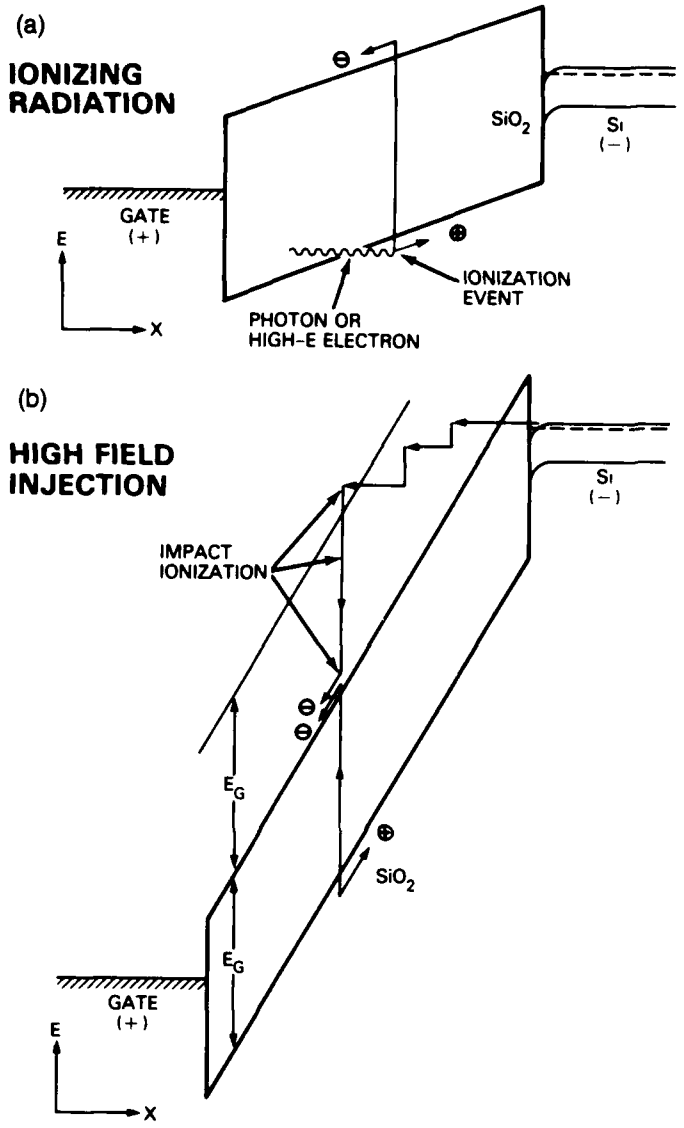

Figure 1. Creation of electron/hole pairs in SiO_2 (a) by penetrating ionizing radiation, and (b) via impact ionization by electrons injected into SiO_2 by Fowler-Nordheim tunneling under large applied field.

These ionization events occur essentially uniformly through the bulk of the SiO_2. The probability, P, that an injected electron will create an electron/hole pair is given by the expression

$$P = L\alpha_o \exp(-H/E) \quad , \tag{2}$$

where α_o and H are constants and L is the oxide thickness. Solomon obtained $\alpha_o = 6.5 \times 10^{11}$ cm^{-1} and H = 180 MV/cm by fitting this expression to his data [9]. P is plotted in figure 2 for an oxide thickness of 100 nm. Impact ionization becomes a practical process for oxide fields greater than 8 MV/cm.

The area density, Q_{Ai}, of holes created by impact ionization in the SiO_2 is given by the product of the injection current (J), the ionization probability (α), the oxide thickness (L), and the duration of the injection (Δt):

$$Q_{Ai} = J\alpha L\Delta t$$
$$= \alpha_o AL\Delta t \exp[-(H + B)/E] \quad . \tag{3}$$

The area density, Q_{Ar}, of holes created in SiO_2 by ionizing radiation is described by the following expression:

$$Q_{Ar} = KLf(E)D \tag{4}$$

where

$$K = 1.22 \times 10^{-6}\ C \cdot cm^{-3} rad(SiO_2)^{-1}$$

is the infinite-field ionization coefficient and D is the absorbed dose in the SiO_2 (rad(SiO_2)); f(E) is a field-dependent charge yield parameter and has the value 0.83 at E = 1 MV/cm for high-energy irradiation (e.g., ^{60}Co) [12]. Therefore, in order to determine the equivalent "dose," D_{eq}, delivered to an SiO_2 gate oxide by the impact ionization technique, the created hole densities from impact ionization and ionizing radiation (eq (3) and (4)) are equated, and the resulting expression solved for D:

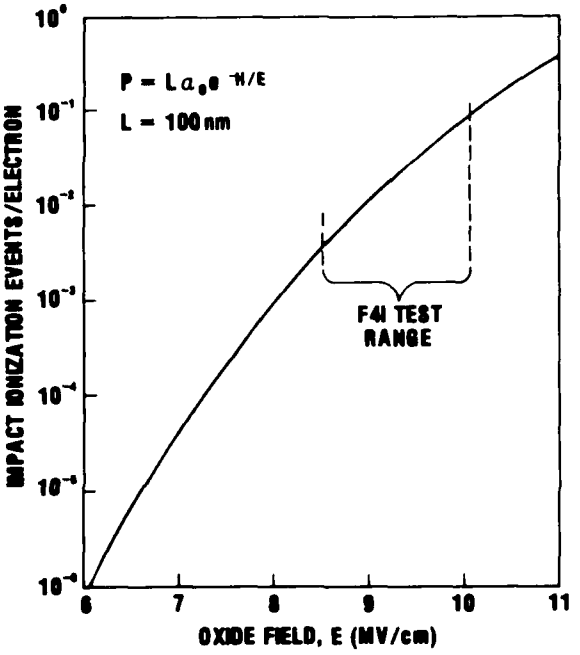

Figure 2. Probability of an impact ionization event per electron as a function of oxide field in a 100-nm oxide.

$$D_{eq} = [\alpha_o AE^2\Delta t/Kf(E)] \exp(-H + B)/E \quad . \tag{5}$$

Using the approximate values for the parameters discussed previously, we can estimate the equivalent dose due to impact ionization:

$$D_{eq} \sim 10^{24} E^2 \Delta t \exp(-418/E) \tag{6}$$

where E is expressed in megavolts per centimeter. For E = 9 MV/cm, equation (6) yields $D_{eq} \sim 10^6 \Delta t$. Thus, applying a field of 9 MV/cm in pulses for a total of 1 s should introduce as many holes into the SiO_2 as a 1-Mrad(SiO_2) irradiation under 1-MV/cm applied field.

The equivalent dose may also be expressed in terms of the injected electron fluence, Q_I, where $Q_I = j\Delta t$.

$$D_{eq} = [\alpha_o/Kf(e)]Q_I \exp(-H/E) \tag{7}$$
$$= 6 \times 10^{17} Q_I \exp(-180/E) \quad . \tag{8}$$

3. REVIEW OF EARLY EXPERIMENTS WITH F4I TECHNIQUE

3.1 Test Circuit and Measurement Procedure

A simplified schematic of the circuit used to apply the F4I test is shown in figure 3a, and a block diagram of the apparatus used for the early measurements is shown in figure 4. The general arrangement was similar to that employed by Shatzkes and Av-Ron for their impact ionization studies [11]. In our case, a generator produced positive rectangular pulses of variable duration, Δt, and repetition rate. These pulses were amplified to the desired amplitude (typically 50 to 100 V) in an output stage designed for close amplitude control and pulse top flatness. The pulses (V_p in fig. 3a) were added to an adjustable background bias voltage, V_B, and were applied to the gate electrode of the MOS sample. The current, I, flowing through the MOS capacitor was converted to a voltage by a fast operational amplifier and the current pulses were displayed on an oscilloscope. The current, I_I, injected into the sample was read from the oscilloscope trace at a time, Δt_m, long enough after the start of the voltage pulse for the much larger displacement current from the charging of the sample capacitance to have died out. The amplitude, V_I, of the injection pulse was also accurately measured at this time using a fast sample-and-hold/analog-to-digital converter system synchronized to the injection pulses. Following pulsed injection, the MOS sample

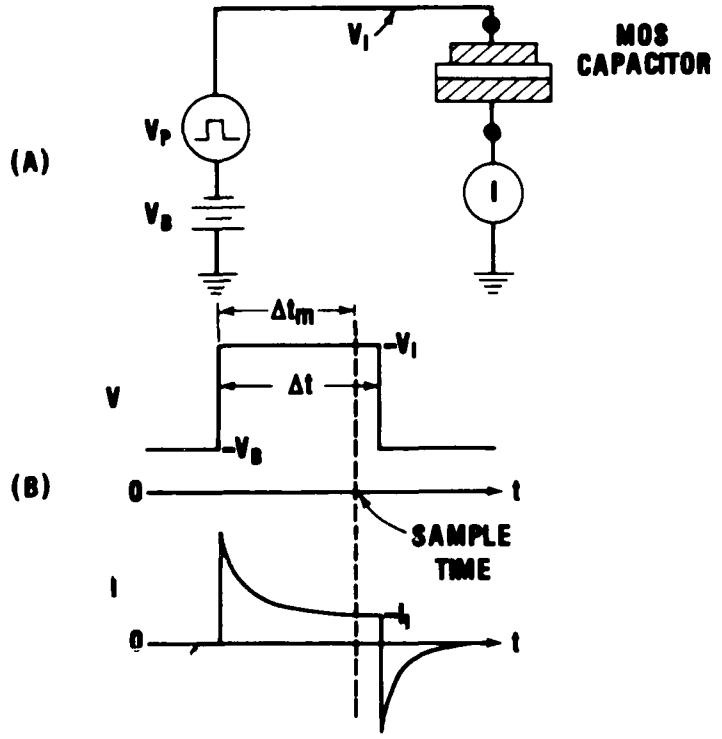

Figure 3. Schematic of F4I test: (a) simplified circuit and (b) sample voltage and current waveforms during an injection pulse.

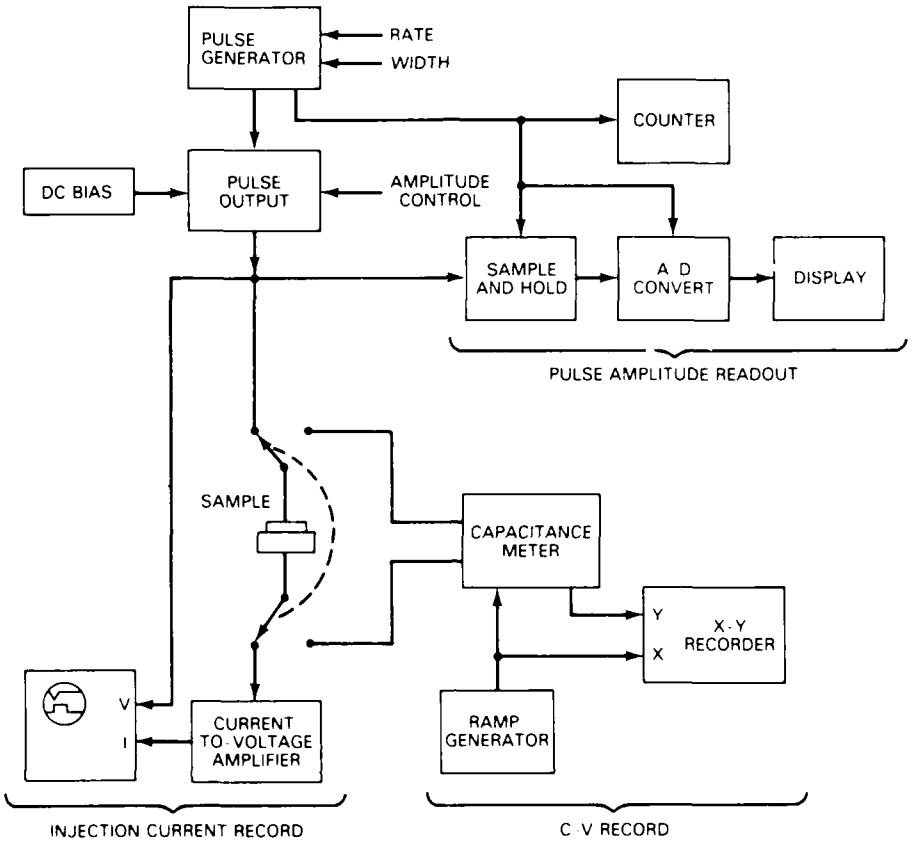

Figure 4. Block diagram of circuit used for early F41 measurements.

was switched to a standard C-V characteristic measurement system to record the effects of the injection. Primary considerations in the experimental design were that (1) the stressing pulses must be fairly short (microseconds to milliseconds) to minimize current runaway to breakdown; (2) the pulse amplitude must be accurately controlled and measured because of the strong field dependence of the injection and impact ionization processes; and (3) the injection pulse must be flat topped, and the current amplifier must recover rapidly from overloads to simplify injection current measurements in the presence of large transient displacement currents in the sample.

In a typical measurement sequence, the injection pulse amplitude was first preset to a voltage corresponding to the desired applied electric field, and the pulse duration was set. A number of injection pulses were then delivered to the sample, and the average injection current was monitored. (Trapping of holes near the SiO_2/Si interface generally caused some increase in the injection current as the pulsing progressed because of enhancement of the field at the interface. This trapping of holes would have little effect

on the field in the SiO_2 bulk and, consequently, upon the electron/hole pair creation rate.) When the desired injected electron fluence was reached, the pulsing was stopped, and the C-V characteristics of the sample were measured.

3.2 MOS Samples for Early Experiments

To show that the F4I technique could be used to assess the hardness of MOS structures, various MOS gate materials were tested. They were obtained from several different suppliers and represent different processes and levels of radiation hardness. SD oxide was a commercial type, thermally grown in dry oxygen; D was a moderately radiation-tolerant, dry-grown oxide; HD was a radiation-hard dry-grown oxide; and HW and TW were hard, pyrogenic-H_2O, wet-grown oxides. The wet oxides were grown at temperatures from 850 to 950°C and annealed at the same temperatures used for the growth.

The dry oxides were grown at 1000°C and were not annealed. All the SiO_2 layers were grown on 1 to 5 Ω-cm n-type Si. The samples all employed aluminum gate electrodes that were vapor deposited from carbon crucible or electron-beam-heated sources and that were sintered at 500°C in argon or nitrogen for 15 to 20 min. For our tests, the MOS capacitors were mounted on TO5 headers. Mounting is not essential for the F4I test, but was done in this case to facilitate the irradiation of some capacitors of each type at the ^{60}Co source. Preirradiation bias-temperature measurements showed very small effects in all the samples in these tests. Oxide layer thicknesses were determined by ellipsometry or capacitance measurements.

3.3 Fowler-Nordheim Tunneling

Samples of each type of MOS capacitor were measured to determine the dependence of oxide current density, J_I, upon applied electric field, E. Voltage pulses of increasing magnitude were applied to each sample and the injection current, I_I, was measured as described above. Figure 5 shows Fowler-Nordheim plots (J_I/E^2 as a function of 1/E) for the various samples. (We assumed that impact ionization made a negligible contribution to the measured sample current. As shown by figure 2, this was certainly true for all but the highest field points.) The highly linear relationships on this plot strongly imply that Fowler-Nordheim tunneling was the dominant charge injection process as expected. At 1/E = 0.11 cm/MV (i.e., 9 MV/cm applied field), the curves for the various samples show a spread of about a decade in V_I/E^2. In principle, these curves should be coincident. The variations between sample types may have resulted from variations in the tunneling barrier heights due to details of the SiO_2/Si interface. In addition, slight errors in the electric field, E, at the interface can shift the curves significantly. In the present case, E was calculated directly from the applied voltage, V_I, and the oxide thickness, L, both of which are subject to measurement error. In addition, the actual interface electric field is perturbed by fixed oxide charge and interface states. Without taking these factors into account, a fit to the mean of the data in figure 5 yields values for the Fowler-Nordheim tunneling parameters of $A = 5 \times 10^5$ A/MV² and B = 221 MV/cm, in reasonable agreement with results from other investigators.

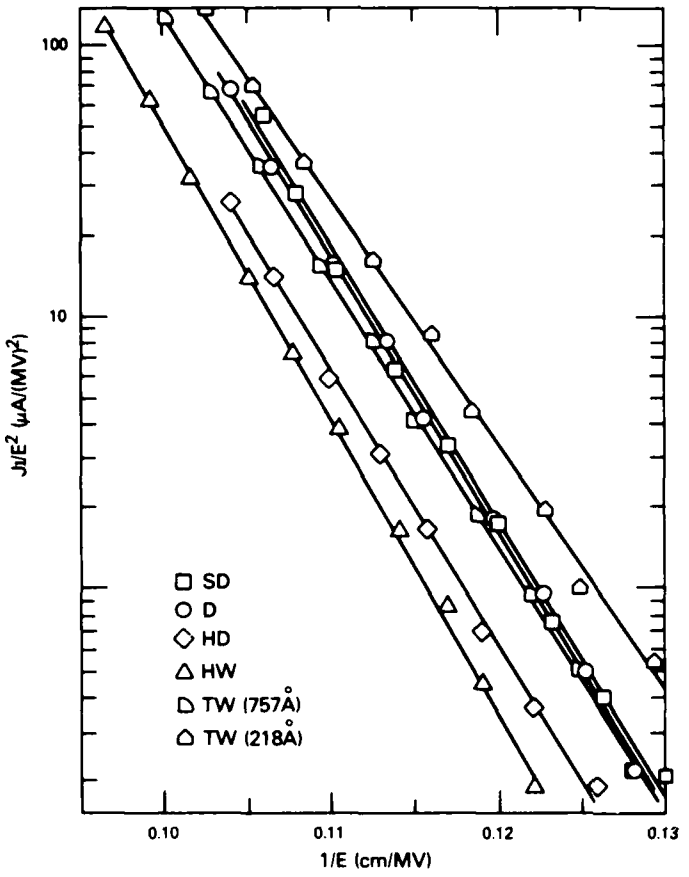

Figure 5. Fowler-Nordheim plots (J_I/E^2 as a function of 1/E) for various MOS capacitor samples measured using F4I apparatus.

3.4 Comparison of F4I Test Effects with ^{60}Co Irradiation

Figure 6a shows the effect of irradiation of a TW sample with an oxide thickness of 75.7 nm under 1-MV/cm positive bias to doses of 2×10^4 and 10^5 rad(SiO_2) in the HDL ^{60}Co source. Note the progressive negative shift and increasing distortion (stretchout) of the C-V curves with increasing dose. The negative shift is associated with net positive charge trapping (holes) in the oxide, while the curve distortion is generally attributed to radiation-induced interface-state buildup.

Figure 6b shows the response of a 75.7-nm wet oxide (TW) capacitor to various levels of total injected electron fluence at 9.5 MV/cm. Comparison of figures 6a and 6b shows that electron injection and ^{60}Co irradiation produced changes in the C-V curves that were qualitatively similar, with comparable negative ΔV_{FB} and stretchout.

To determine quantitatively the correlation between the effects of the F4I technique and ionizing radiation on the MOS capacitors, the various types of samples were irradiated at the HDL ^{60}Co facility to doses of 10^4 to 10^5 rad(SiO_2). Similar samples were exposed to F4I injection at 9 MV/cm and

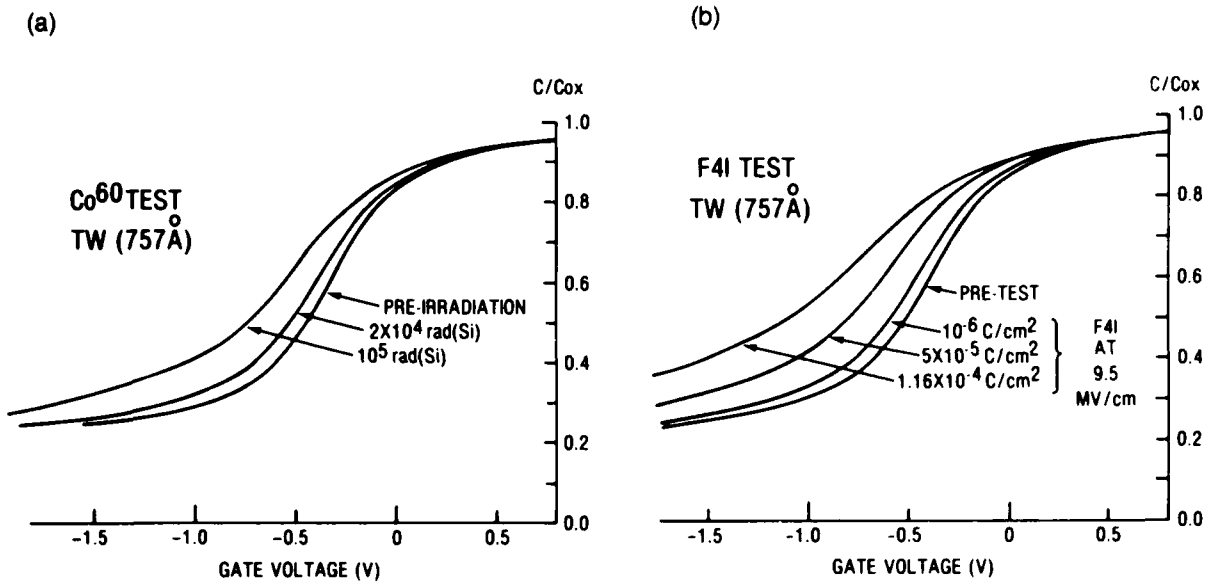

Figure 6. Capacitance-voltage characteristics for 76-nm oxide samples: (a) before and after irradiation in a ^{60}Co source and (b) before and after high-field electron injection (F4I technique) at 9.5 MV/cm to various electron fluences.

for equal injected electron fluences (1.9×10^{-5} C/cm^2). (Both the ^{60}Co total dose and injected electron fluence levels were kept low to keep the resulting flatband shifts in the relatively linear damage region below 10^5 rad(SiO_2).) In order to compare the results properly, the ^{60}Co flatband shifts were first normalized to a uniform 10-krad(SiO_2) dose. Then, in order to compare results for the various oxide thicknesses on an equal footing, both the F4I and ^{60}Co results were normalized to an equivalent 100-nm oxide thickness assuming an oxide-thickness-squared dependence [12]. The results are plotted in figure 7. The data are readily fit by a straight line, indicating that the damage introduced by the F4I technique "tracks" the damage produced by the ^{60}Co irradiations. From the slope of the line, an injected electron fluence of 1.9×10^{-5} C/cm^2 at 9 MV/cm was found to be 2.3 times as effective at introducing incremental ΔV_{FB} as the 10-krad(SiO_2) ^{60}Co irradiation. Thus, the experimentally determined relationship between injected charge $Q_I = J_I \Delta t$ at 9 MV/cm and equivalent dose D_{eq} was found to be given by

$$D_{eq} = 1.2 \times 10^9 \, Q_I \quad . \tag{9}$$

In a typical sample, J_I at 9 MV/cm was ~10^{-3} A/cm^2, so that $D_{eq} \sim 10^6 \Delta t$, in agreement with the estimate of equation (6) for a field of 9 MV/cm.

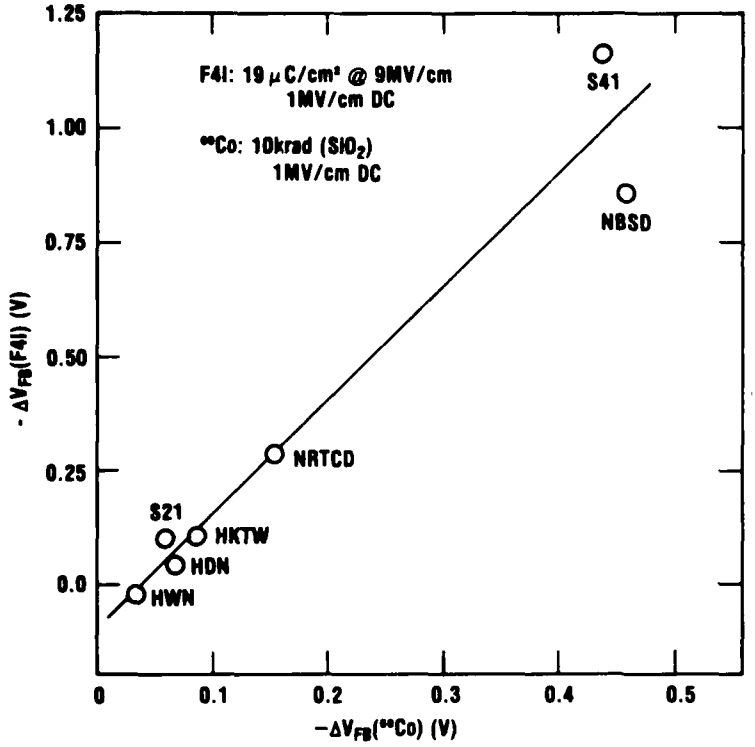

Figure 7. Normalized ΔV_{FB} produced by high field stressing (F4I technique) to injected electron fluence of 1.9×10^{-5} C/cm² at 9 MV/cm versus normalized ΔV_{FB} produced by 10^4 rad(SiO_2) ^{60}Co irradiation for various MOS samples.

Therefore, within the large uncertainties in some of the parameters, the essential equivalence between hole creation by the F4I technique and by an ionizing radiation source as predicted by equation (5) was verified.

Figure 8 shows C-V curves for 97-nm pyrogenic-oxide MOS samples taken at room temperature (solid curves) and at 77 K (dashed curves) before and after F4I test exposure. Note that the room-temperature postirradiation C-V curve shows significant distortion (stretchout) with respect to the room-temperature pre-irradiation curve, while the 77 K post- and pre-irradiation curves show little change in shape. At room temperature, the charge in interface states can respond to changes in the gate voltage and cause distortion in the C-V curves, whereas at 77 K the interface-state charge is "frozen in" in the interface states and does not affect the shape of the C-V curves. Therefore, the observed increase in distortion in the room-temperature C-V curves for this sample is attributable to generation of interface states rather than other possible sources of distortion such as a laterally nonuniform buildup of oxide trapped charge.

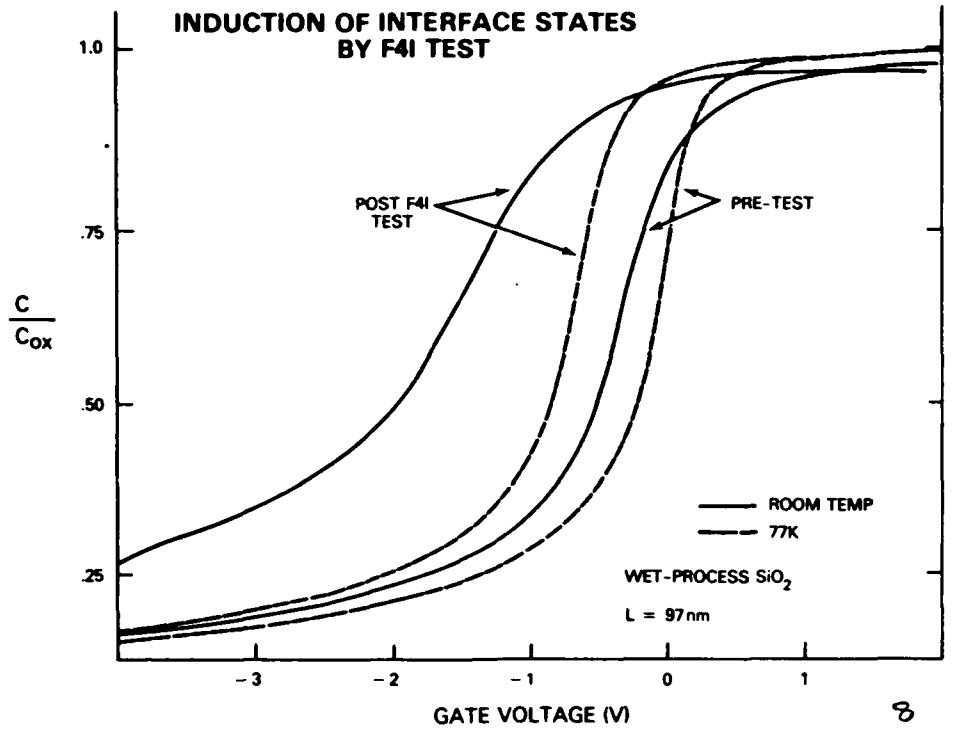

Figure 8. Capacitance-voltage characteristics for 97-nm wet-process MOS oxide sample measured at room temperature (295 K) and 77 K before and after high-field stressing (F4I test).

4. DIELECTRIC BREAKDOWN IN SiO_2 SAMPLES

4.1 Background

The electric field applied across the SiO_2 layer during an F4I test sequence is typically in the range from 8.5 to 10 MV/cm, corresponding to 85 to 100 V across a 100-nm oxide. Such fields/potentials are far greater than those normally applied to MOS structures and consequently dielectric breakdown might be anticipated. In fact, the intrinsic breakdown field of SiO_2 is much greater than 10 MV/cm and may be as high as 30 MV/cm [13]. Nevertheless, dielectric breakdown almost universally occurs within a fraction of a second in apparently fault-free MOS structures stressed with steady (not pulsed) fields above about 8 MV/cm. Considerable work has been done on breakdown (see review [14]); typically a "runaway-to-breakdown" phenomenon is observed. When the electric field is first applied, an apparently normal and constant Fowler-Nordheim tunneling current is initially measured. Suddenly, after a fraction of a second, a rapidly but smoothly increasing current is observed, followed generally by current "spikes," permanent sample breakdown, and shorting. One model [15] for this process suggests that electron injection via tunneling into the oxide takes place preferentially at thinner spots in the dielectric where higher electric fields may be present. Impact ionization would then also take place preferentially at these locations. The excess impact-generated holes "decorating" the defect region enhance the electric field in

that region at the interface, resulting in an additional local increase in electron injection. This process is therefore regenerative and can "run away" to oxide damage and breakdown.

4.2 Breakdown under F4I Test Conditions

The F4I test technique avoids dielectric breakdown in most MOS samples by applying high electric fields across the SiO_2 in short pulses rather than in a continuous (dc) manner. For typical test conditions the injection pulse duration may be tens of microseconds with a duty cycle of a few percentage points. Applying the high field in this manner prevents injection current runaway to breakdown in most cases. In terms of the breakdown model outlined above, applying the electric field in short pulses would probably have the effect of choking off the incipient runaway process. As discussed in the introduction, holes move slowly. Most of the small number of excess holes generated in a defect region during a short injection pulse may have time to transport away from the region during the relatively long low-field interval before the next pulse. Thus, local amplification of the interface electric field would be reduced and, with it, the tendency toward positive feedback and breakdown.

The F4I test has been successfully applied to most of a wide variety of MOS capacitor samples at our laboratory. However, as may be expected, sample failure by dielectric breakdown did occur frequently before useful test results could be obtained. The rate of failure was highly dependent upon sample type: in certain batches of samples perhaps only 1 in 10 would break down under the test conditions; on the other hand, a few sample types were never successfully tested (~20 samples of these types were tried). No clear correlation between sample dielectric strength and the known oxide processing differences (e.g., wet or dry oxidation, annealing schedules) was evident. Most of the failures occurred immediately upon application of a test voltage staircase at relatively low fields, suggesting the presence of gross defects such as spikes (local metallization intrusions into the SiO_2).

4.3 Examination of Early Breakdown in F4I Samples

Dielectric breakdown was studied in detail in several representative MOS capacitor sample lots. The samples were subjected to short voltage pulses of slowly increasing amplitude (pulse voltage staircase) using the prototype F4I apparatus. The apparatus was programmed to continuously monitor the injection current through the sample, and signal and halt the pulse voltage staircase when excessive current flow (usually above a few microamperes per square centimeter) was detected. When this occurred, the test was repeated to confirm the failure. Most frequently, excessive current would then be measured upon application of the first pulse at a very low voltage, indicating that the sample had sustained permanent damage (shorted). Often, however, upon retest, samples did not register excessive current at the previous voltage levels and either passed the test (i.e., sustained voltage pulses corresponding to a field of 10 MV/cm without shorting), or developed permanent damage at a higher voltage than the initial failure level. This "healing" effect sometimes occurred several times in a sample at successively higher

voltages, and might be attributed to burnout of conductive paths such as metallic filaments through the oxide. In any case, the breakdown field for this test was defined as the applied field at which permanent (nonhealable) damage occurred.

Figure 9 shows breakdown distributions obtained for representative "weak" and "strong" MOS capacitor lots. The applied electric field range from 0 to 10 MV/cm was divided into intervals (bins) and the number of samples that broke down within each field interval is plotted as a histogram over these intervals. The "weak" samples failed most frequently at very low fields, well below the onset of measurable Fowler-Nordheim tunneling. The "strong" samples showed only a few scattered failures at fields below 8 MV/cm. This study again showed no obvious correlation of "strong" or "weak" breakdown characteristics with oxide processing (supplier, wet or dry oxide growth, annealing schedule). Instead, several instances were found in which MOS capacitors from the same process lot but which were mounted and bonded at different times showed markedly different breakdown distributions. At that time, most F4I measurements were performed on samples mounted on headers to facilitate concurrent ^{60}Co tests rather than directly on wafers with a probe station. When samples from these lots were tested for breakdown directly on the wafer using a probe station, most of the samples survived stressing to 10 MV/cm. Evidently the sample mounting/bonding process was responsible for most of the observed differences in breakdown behavior. The samples used for these tests were

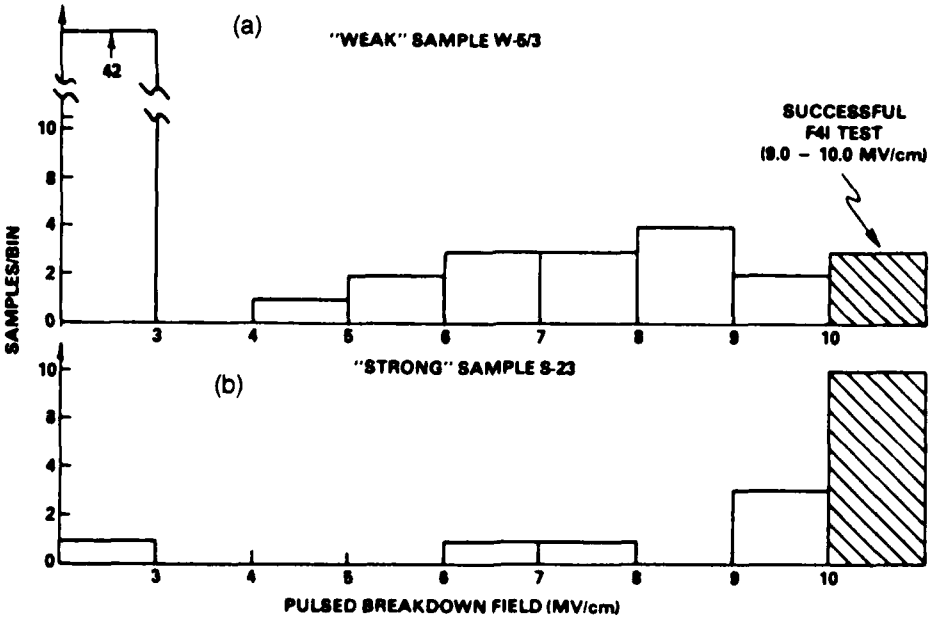

Figure 9. Distribution of oxide dielectric breakdown (hard short) voltages for MOS capacitor samples under pulsed gate voltage: (a) "weak" oxide samples and (b) "strong" oxide samples.

simple MOS capacitor dots consisting only of the Si substrate with a uniform thin oxide grown upon it and a vapor-deposited Al electrode. The electrode contact was formed by thermocompression bonding the gold lead wire onto the Al directly over the thin oxide. Apparently certain bonding conditions, while not producing directly shorted samples, resulted in damage to the oxide, with subsequent low-voltage breakdown.

4.4 Improved Test Structures

As originally envisioned, the F4I test would typically be applied by an IC manufacturer as a wafer-level check on the radiation hardness of his product as it comes off the process line. In this mode, the samples to be tested would probably be drop-in or on-chip test structures on a fully processed multimasked wafer rather than simple capacitor dots. To avoid damage to the thin oxide to be tested, the F4I test structures might employ bonding or probe pads on the relatively thick field oxide. To check this and to support more recent in-house testing using the F4I technique, a simple Al-gate MOS capacitor test chip using two mask levels was designed. Wafers were fabricated using this mask set and the resulting capacitors showed generally good breakdown characteristics (fig. 10) whether they were tested on the probe station or after being mounted on headers and wire-bonded.

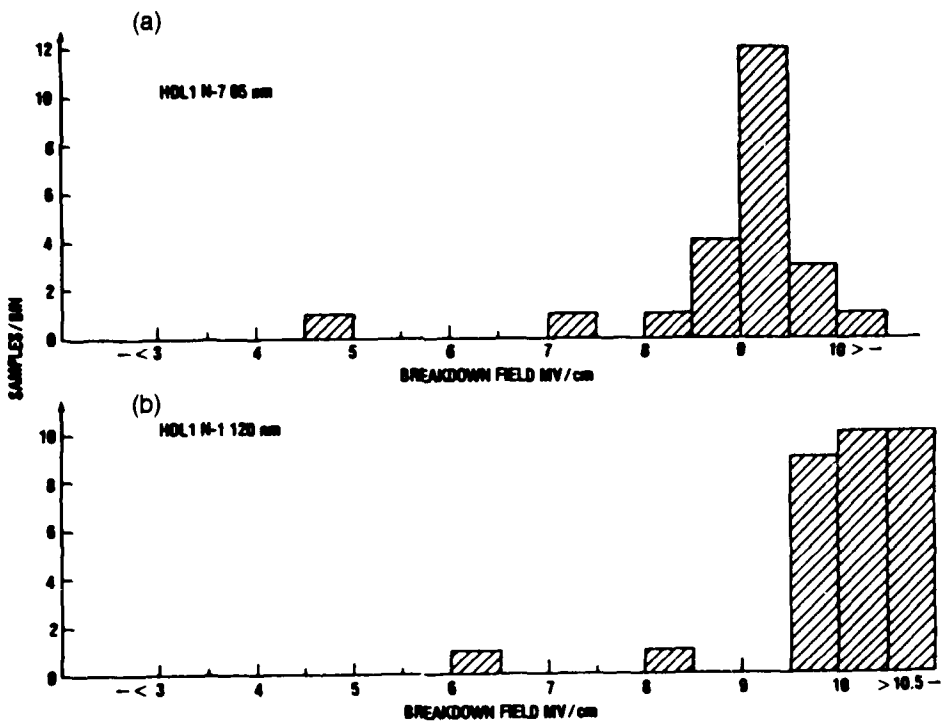

Figure 10. Distributions of oxide dielectric breakdown voltages for two types of MOS capacitor samples with improved design: (a) 65-nm samples and (b) 120-nm samples.

4.5 Delayed Breakdown (Wearout)

An MOS capacitor sample which passed the voltage staircase breakdown test to 10 MV/cm could generally be successfully injected to moderate electron fluences (~10^{-4} C/cm^2) at ~9 MV/cm (equivalent doses ~10^5 rad(SiO_2)). However, dielectric breakdown almost invariably occurred in all types of samples before an electron fluence of 10^{-2} C/cm^2 at 9 MV/cm was reached (~10 Mrad(SiO_2) equivalent dose). This "wearout" process has been observed by others and has been attributed variously to an accumulation of deeply trapped impact-ionization-generated holes in the oxide, or cumulative oxide damage by the injected electron flux, or a combination of these [16, 13]. In any case, this process appears to place an upper, but clearly not stringent, limit on the use of the F4I test.

5. DEVELOPMENT OF A PROTOTYPE F4I TEST SYSTEM

5.1 Desired Test System Characteristics

The experimental apparatus shown in figure 2 was adequate for the initial experiments, which verified the Fowler-Nordheim tunneling and impact ionization processes in several types of MOS capacitors and demonstrated that results from application of the F4I test correlated with ^{60}Co radiation damage to these capacitors. However, this apparatus was not suitable for routine testing of MOS samples for radiation response prediction or hardness assurance purposes. A typical test run required calculation and manual setting of injection pulse amplitude and "eyeball" measurement of pulse duration with an oscilloscope, constant monitoring and measurement of injection current with an oscilloscope (again "by eyeball") during the injection process, hand calculation of total electron fluence, and manual termination of the injection when the proper fluence was reached. To facilitate application of the F4I test, the following features were considered desirable for a practical test system:

(1) accurate (preferably digital) readout of all important test parameters (injection voltage, pulse duration, injection current);

(2) continuous calculation of total injected charge and sensing of the test endpoint (when the desired total charge injection is reached);

(3) continuous monitoring of test parameters to detect and signal faults (e.g., error in injection voltage, readings out of range, sample short);

(4) prompting of operator in test sequence, including calculation of test conditions from sample parameters and desired equivalent dose; and

(5) sufficiently fast operation of apparatus to allow completion of a typical test cycle within a few seconds or minutes.

5.2 Design of Prototype System

The desired system features clearly require a "smart" test system, which in turn dictates a system configured around a computer or controller. Two approaches toward building such a system were considered. First, a test set might be constructed using standard commercial instruments controlled by a mini- or microcomputer through a standard input/output (I/O) interface (RS232 serial or GPIB (IEEE Standard 488) parallel). Second, custom test circuits could be designed and interfaced directly with the microcomputer through its data and address buses. The first approach, if usable, would probably be most quickly applied and cost-effective for potential users of the F4I test, since the purchase or use of on-hand standard instruments is generally faster and less expensive than in-house construction of circuits from the component level. Unfortunately, it became clear that the identified requirements of the F4I apparatus could not be met with then-existing off-the-shelf instruments. Neither a voltage- nor a current-reading instrument with the required fast sample-and-hold, readout, and fast recycle capabilities was available. Also, a system based on either the RS232 or GPIB communications standards would be severely limited in speed of operation, since continuous high-speed two-way communications were required for monitoring of injection conditions on each pulse.

5.2.1 Hardware Description

The F4I test system configuration decided upon was primarily a series of custom-designed and locally constructed modules or circuits which communicated with a microcomputer controller via direct parallel interfaces to the microcomputer's data and address buses. *Figure 11 shows a block diagram* of the prototype F4I test system. The microcomputer, under program control and with operator input, sets up sample injection voltage via a digital-to-analog converter (PULSE SET D-A) and commands pulse output through a timing logic circuit. The timing circuit triggers the pulse generator and, at a preset time, t_m, into the injection pulse, triggers sampling and digitization of both the injection voltage (READBACK D-A) and injection current (I-V AMP and CURRENT A-D). (Refer to fig. 3.) The timing logic also controls operation of a circuit which measures the effective duration of the injection pulse (PULSE Δt COUNTER). MOS sample condition is measured with a C-V system consisting of a 1-MHz capacitance meter, 10-s voltage ramp generator, and an X-Y recorder.

The controller chosen (in 1980) for the F4I system was the Apple II, an inexpensive "personal" microcomputer employing an 8-bit 6502 microprocessor with 48-kilobyte random access memory, 5-1/4-in. floppy disk drive program/ data storage, and CRT/keyboard operating console. This unit was chosen for its low cost, general availability, and convenient programmability in both BASIC and microprocessor assembly languages. (At the time, the Apple II was unique in these respects.) The Apple II accepted plugin cards through a series of peripheral connectors which allowed direct access to the microcomputer's data and address buses and certain control lines. Either simple custom-built or inexpensive commercial plugin cards (e.g., Electronics World EW-1100) or simple parallel input and output data latches were employed to interface the Apple II to the various test system modules.

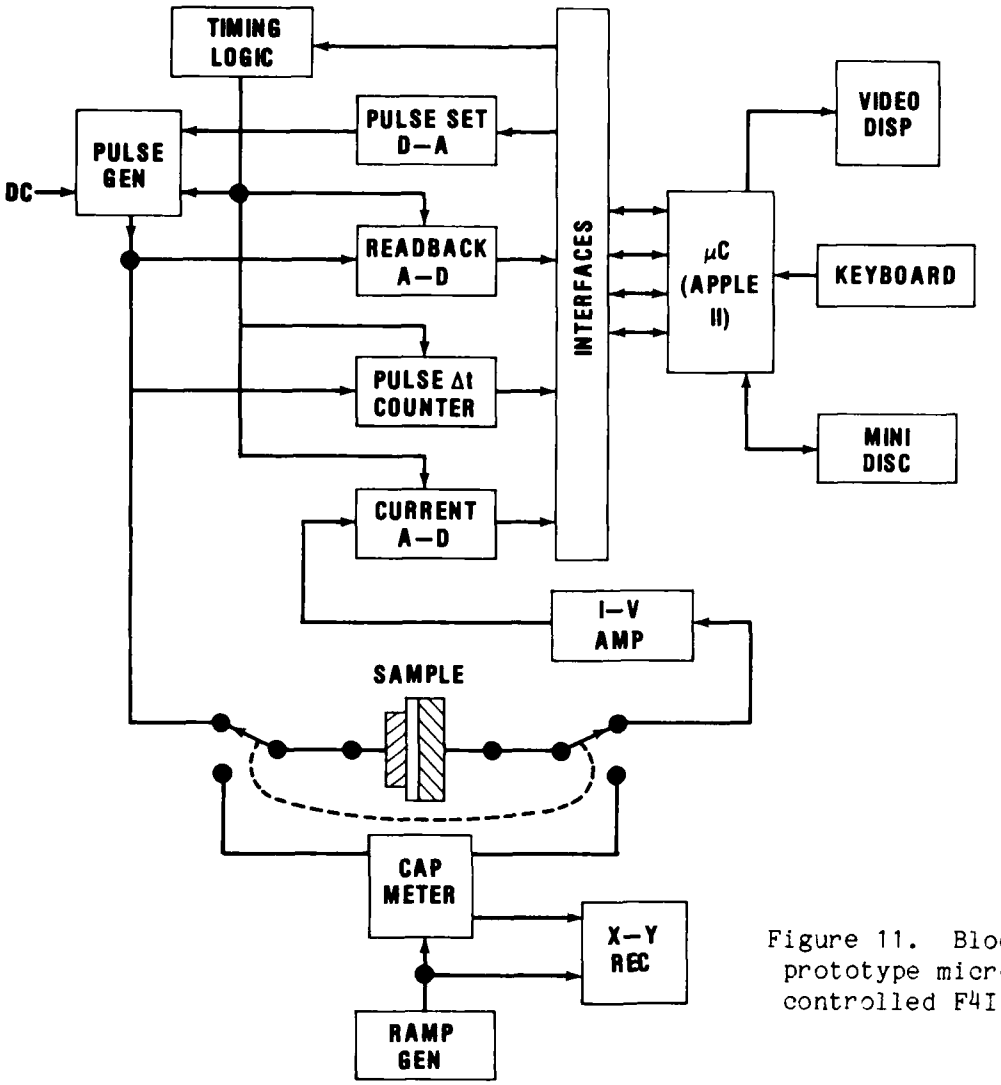

Figure 11. Block diagram of prototype microcomputer-controlled F4I test system.

Circuit diagrams of the major system components that were designed and constructed in-house appear in figures 12 to 16. Figure 12 shows the circuit for the computer-controllable high-voltage pulse generator. Pulse amplitude is preset via a 10-bit word from the microcomputer which is latched into a digital-to-analog (D-A) converter. The 2-mA full-scale output current of the D-A converter is converted to a 10-V full-scale voltage signal which in turn is applied to a high-voltage amplifier module (AD171J) connected for a gain of 15. The output of this unit is a computer-controlled dc level from 0 to 150 V that serves as the positive supply voltage for the pulse output circuit. This output circuit consists of another AD171 module driven in a gain-of-33 configuration by the output of a fast electronic switch. In the quiescent state, the amplifier input is connected to a manually adjustable dc bias source (BACKGROUND DC BIAS). When a pulse trigger is received from the

microcomputer (PULSE TRIG), a pulse with duration set by the WIDTH RANGE and WIDTH VERNIER controls switches the AD171 input to +5 V, overdriving it and causing output of a flat-topped voltage pulse with amplitude determined by its positive supply voltage (i.e., the output of the D-A circuit). The pulse trigger circuit also generates a delayed logic signal (CNVT) that determines the sampling time, t_m, for measuring the pulse amplitude and injection current.

In order to accurately calculate the total injected charge and its equivalent dose, the high-voltage pulse amplitude and its duration and the injected current must be accurately measured. Figure 13 shows the circuit for the analog-to-digital (A-D) converter that is used to read back the amplitude of the high-voltage injection pulses. After 15:1 attenuation, the pulse signal is captured by a fast sample-and-hold module and its amplitude converted to a 10-bit binary word upon receipt of a CNVT signal.

The duration of the high-voltage pulses is measured and digitized by the circuit shown in figure 14. Since the voltage pulse has significant risetime and the injection current and impact ionization is primarily sensitive to the *maximum* applied field, the *effective* duration of the high-voltage pulse is the time at maximum amplitude. Since the voltage pulse is essentially trapezoidal, this is the time between the end of the positive dV/dt on the leading edge of the pulse and the beginning of negative dV/dt on the trailing edge. This time is sensed by the differentiator, amplifier, and logic circuitry in the figure which produces an equivalent-duration HV PULSE LENGTH GATE pulse. The duration of this pulse determines how many cycles of the 7.159-MHz Apple clock signal are gated into the series string of 74193 counters. The resulting count, which is proportional to the high-voltage pulse duration at maximum amplitude, is applied to the Apple interface as a 12-bit binary word.

The injected current through the MOS capacitor is converted to a voltage signal by a fast operational amplifier and is applied to the input (A-D IN) of the circuit shown in figure 15. This circuit scales the input signal and applies it to a sample-and-hold amplifier and 10-bit A-D converter.

The various digital signals from the circuits just described are connected to the Apple II controller through all-purpose interface cards with the circuit shown in figure 16. This circuit consists of an 8255 programmable interface adapter integrated circuit and associated timing and logic circuitry mounted on a circuit board that plugs into the expansion slot connectors on the Apple II. The 8255 is software-configurable to function as an input or output port. As most generally used here, it is configured as two 12-bit ports.

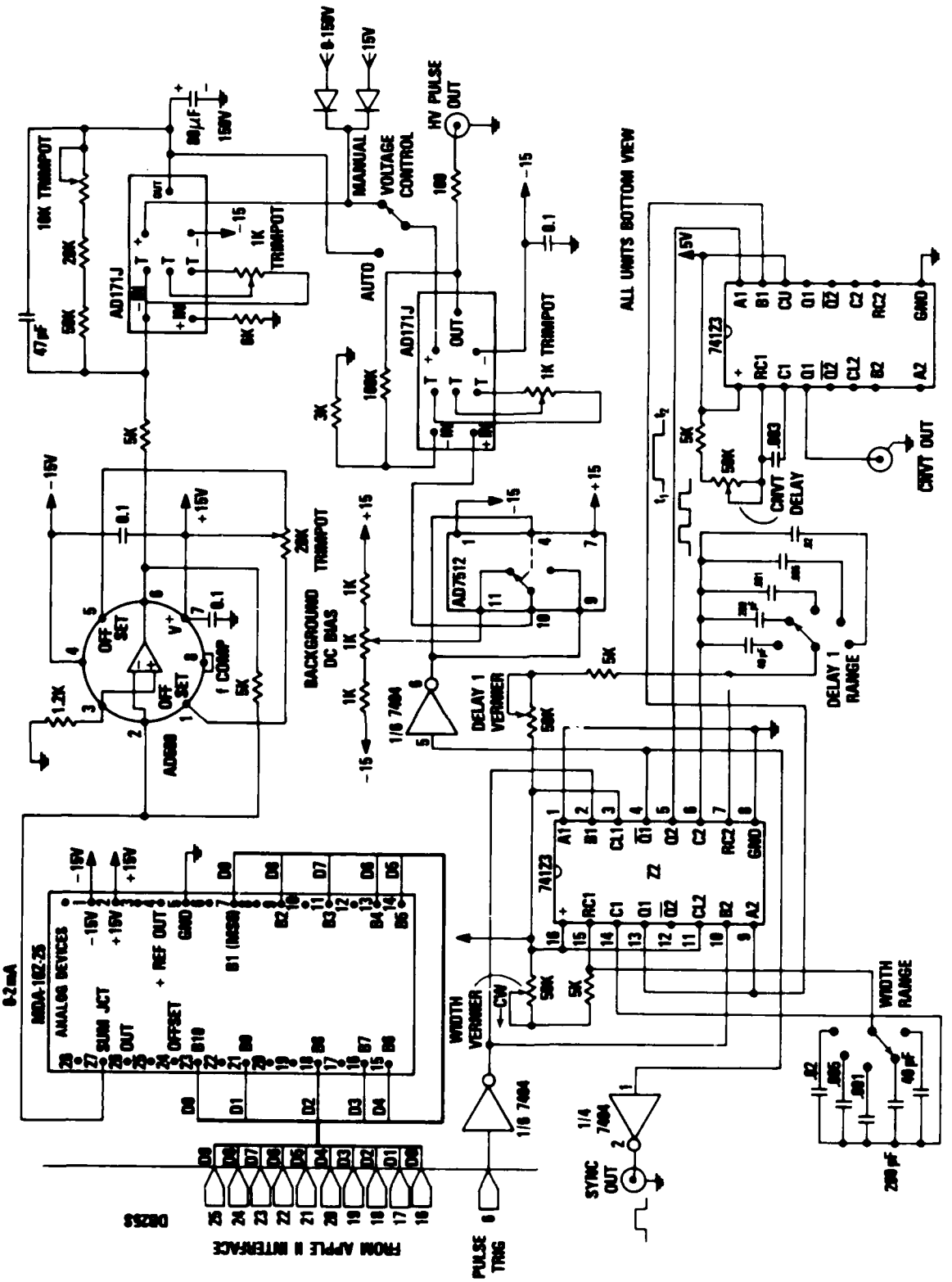

Figure 12. Circuit diagram of computer-controllable high-voltage pulse generator for FHI system.

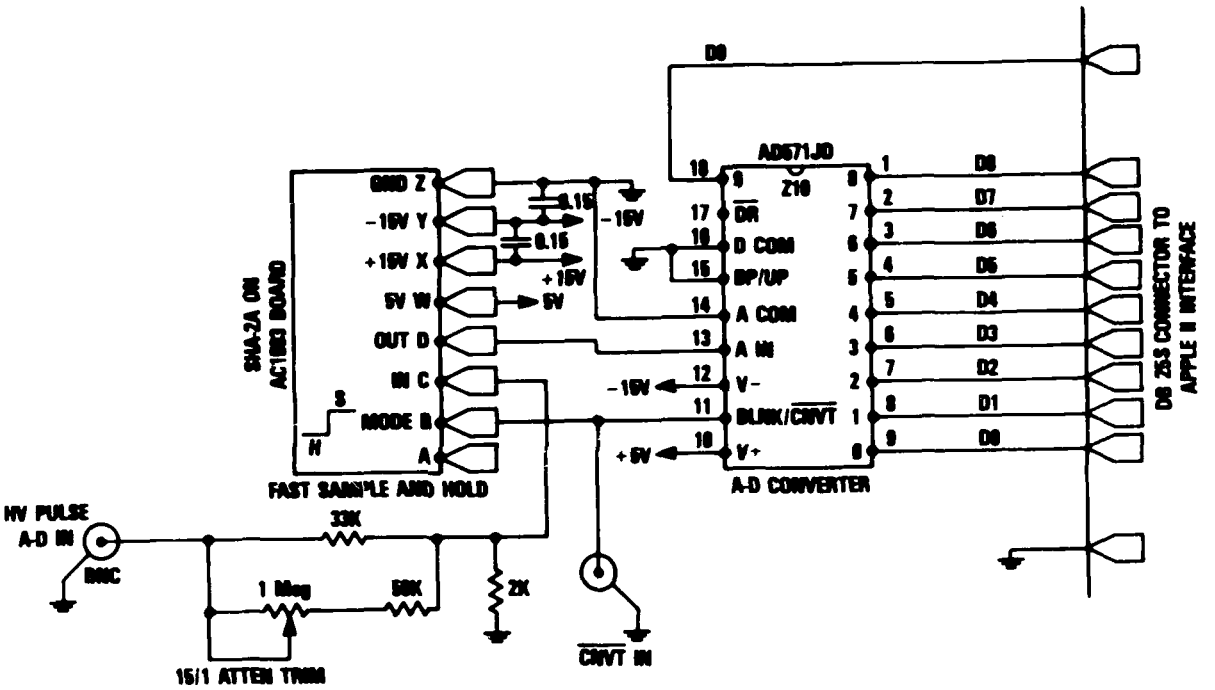

Figure 13. Circuit diagram of analog-to-digital converter to read high-voltage pulse amplitude for F4I system.

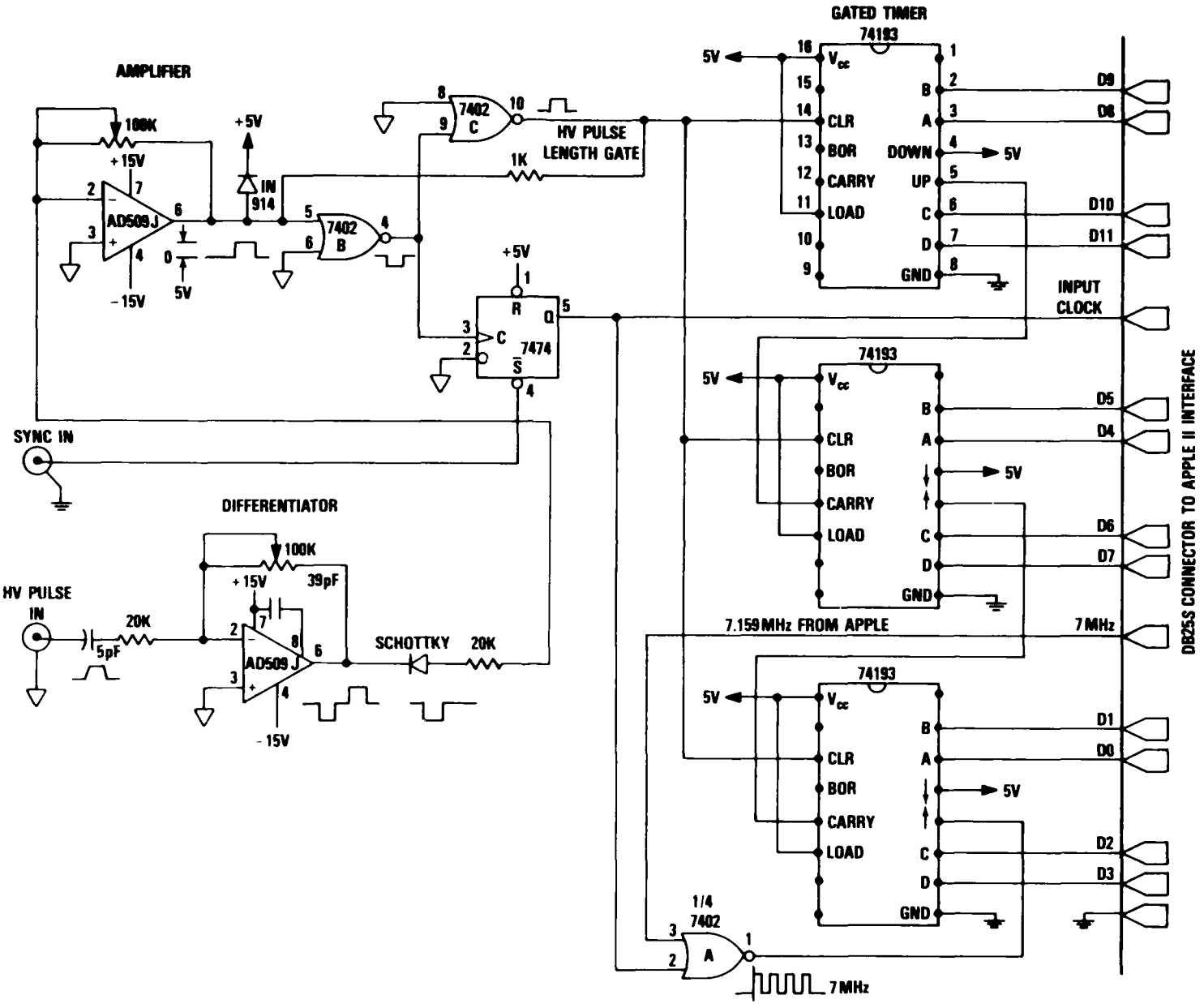

Figure 14. Circuit diagram of logic and timer to measure effective duration of high-voltage pulses for F4I system.

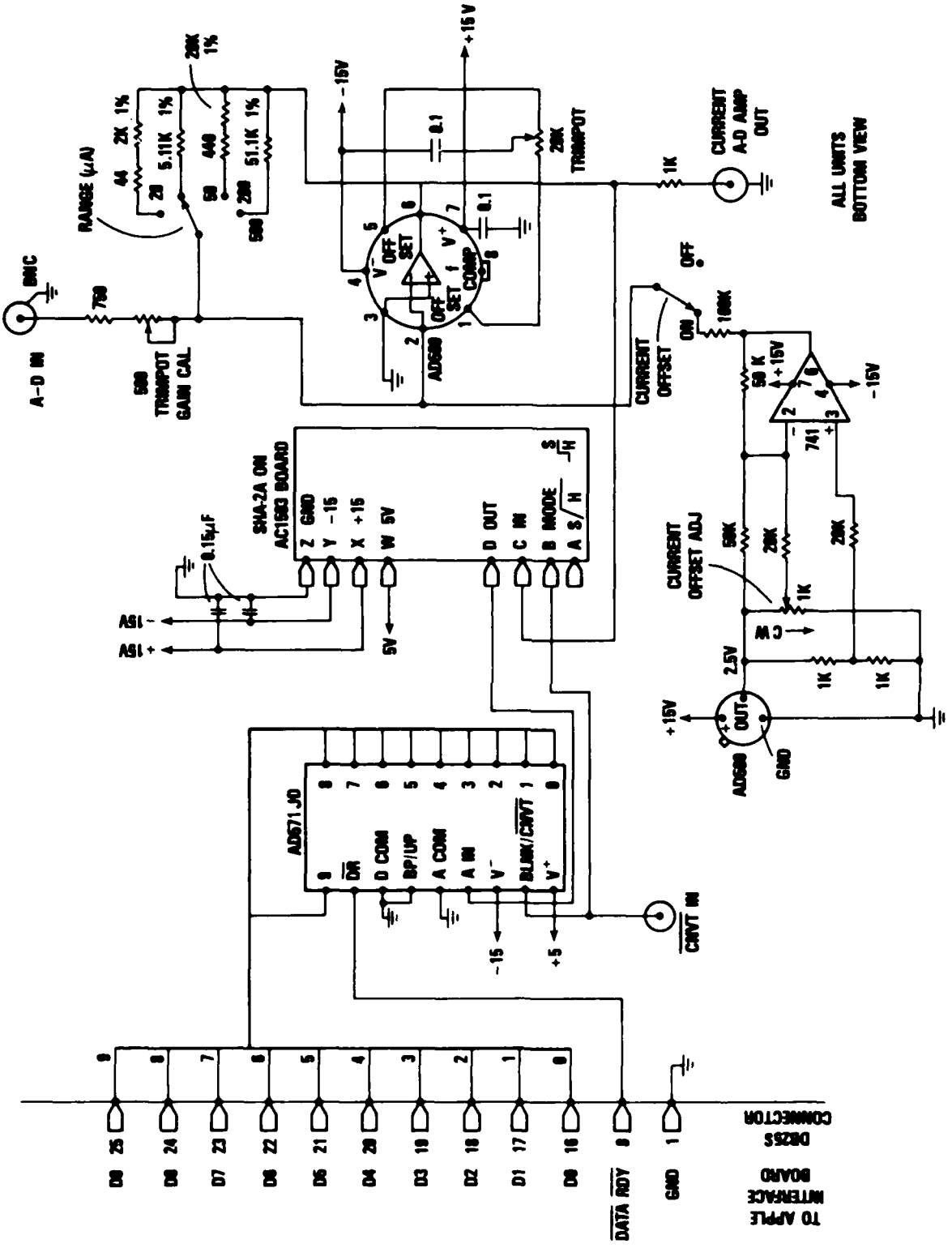

Figure 15. Circuit diagram of injection current sampler for F4I system.

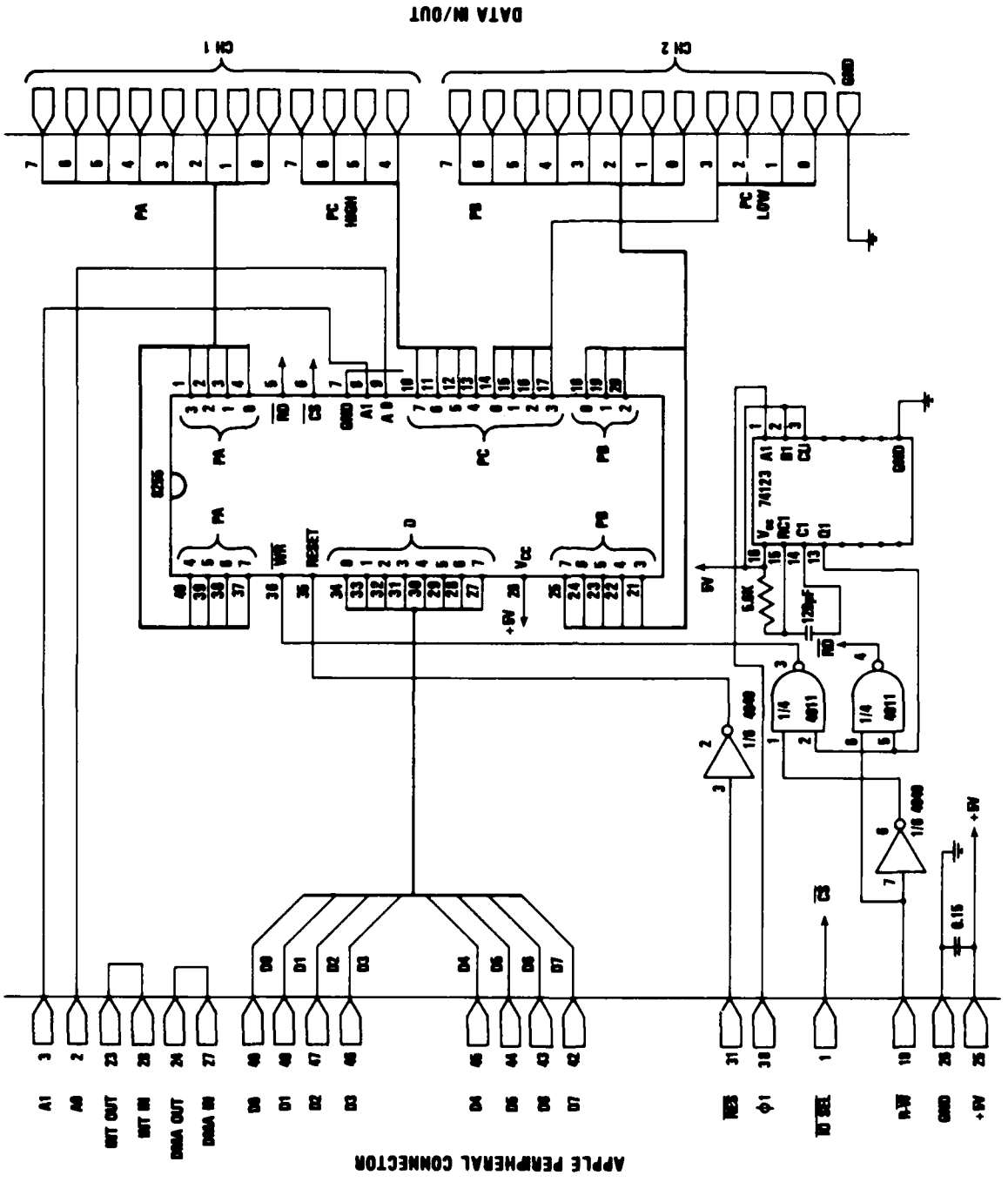

Figure 16. Circuit diagram of general-purpose programmable interface board for coupling digital readouts or controllers to Apple II microcomputer.

5.2.2 Software Description

The software for the Apple II microcomputer to run the F4I tests was written primarily in the Applesoft language, a variant of floating-point BASIC that is supplied with the computer. As an intepreted language, Applesoft BASIC executes fairly slowly; however, this disadvantage was offset, for our purposes, by ease of programming and program debugging and instant availability of the language from read-only memory. Problems with slow execution speed were solved by writing utility routines in 6502 microprocessor assembly language for operations that require fast, repetitive execution or hardware manipulation. These routines were called as necessary from the main BASIC program.

The F4I controller program supports the following operations:

(1) set up and calibrate the test systems;

(2) check MOS capacitor sample for dielectric breakdown;

(3) measure, store, and plot the Fowler-Nordheim (F-N) injection characteristics of a sample;

(4) calculate the oxide thickness of a sample from its F-N characteristics;

(5) calculate the approximate injected charge needed at a particular field on a sample to simulate a desired radiation dose; and

(6) set up and run an injection test sequence to the desired injected charge fluence.

Listings of the main program, F4I TEST.BAS, and its assembly language utility routine, ZAP.COM, appear in appendix A, along with a summary of the main program functional blocks by statement numbers.

5.3 Operation of Prototype System

To illustrate the features of the prototype F4I test system and its operation, a typical test sequence is described here.

With the equipment configured as shown in figure 11, the apparatus is turned on and allowed to warm up (the current amplifiers, in particular, are subject to some thermal drift). The MOS capacitor sample to be measured is positioned on the wafer probing station, and a preliminary C-V curve is run to verify sample integrity and proper electrical contact. The microcomputer is turned on, the disk operating system (DOS 3.3) is booted, and F4I TEST.BAS is run (cold start). The program will ask whether previous system calibration constants, which are stored in a disk file, are to be read in (usually, "yes"). From the main menu, the options available are (1) VOLTAGE RAMP (for sample breakdown check and to generate F-N data on a sample), (2) SAMPLE

INJECTION (to do radiation simulation), (3) PARAMETERS (to read in MOS capacitor data in preparation for Fowler-Nordheim check or radiation simulation), (4) F-N PLOT (to run a Fowler-Nordheim characterization on a sample), (5) ZERO CHECK (to set up zero offset on the current amplifier), and (6) CALIBRATION (to measure and record scale factors for the current amplifier).

Normally a ZERO CHECK is performed first to insure that the current amplifier is properly balanced. This routine asks the operator to select a current range and then repetitively triggers the system at zero injection pulse amplitude and displays the sampled current to allow the operator to adjust the current amplifier/A-D converter for zero indicated current. This routine may also be used to check voltage pulse duration and amplitude and A-D converter timing (CNVT pulse) using an oscilloscope triggered by the SYNC pulse. If the CALIBRATION option is now invoked, the operator may calibrate any or all of the current amplifier ranges by applying known currents from a calibrated current source to the input.

With the equipment properly zeroed and calibrated, the PARAMETERS option is invoked and the MOS sample capacitance and dimensions are input to obtain the oxide thickness and provide the necessary information to calculate the needed injection current per unit area through the oxide. The sample may be checked for premature breakdown or Fowler-Nordheim injection characteristics by invoking the VOLTAGE RAMP option. This procedure applies a series of voltage pulses to the sample, starting at a desired level and increasing by a specified increment to a specified maximum voltage. The injection voltage and current are read at each pulse and their values stored in an array (V_i, I_i). If the injection current exceeds a preset maximum, the pulse sequence is aborted and a message displayed. If the voltage ramp sequence is completed successfully, the (V_i, I_i) array may be saved in a disk file. The Fowler-Nordheim injection characteristic of the capacitor may then be examined by invoking the F-N PLOT option from the main menu. An option (PLOT) from a submenu then allows the operator to display the existing (V_i, I_i) array on a Fowler-Nordheim plot. In the process, the Fowler-Nordheim injection parameters for this capacitor sample are calculated. Other options provide for saving the displayed plot to disk (SAVE PLOT), calling another (V_i, I_i) data set to be plotted (DATA FILE), or determining the oxide thickness (FIT FOR L) from the Fowler-Nordheim characteristic by assuming standard values of the injection parameters (see sect. 3.3). An example of a Fowler-Nordheim plot display appears in figure 17.

To carry out an injection sequence (radiation simulation experiment), the operator would now select the SAMPLE INJECTION option from the main menu. After verifying the sample parameters, the computer asks for the desired current amplifier scale and injection field. It then calculates the required injection voltage and, from the Fowler-Nordheim parameters, the expected injection current and charge needed to produce holes equivalent to a 1-krad(SiO_2) dose. Based on this information, the operator would then select a charge increment for the run. The rate at which pulses are delivered may be varied from about 1 to 500 Hz by specifying the length of two control loops (INNER and OUTER--see the program listing, app A). Upon command, the system then applies injection pulses to the sample. For each pulse the injection

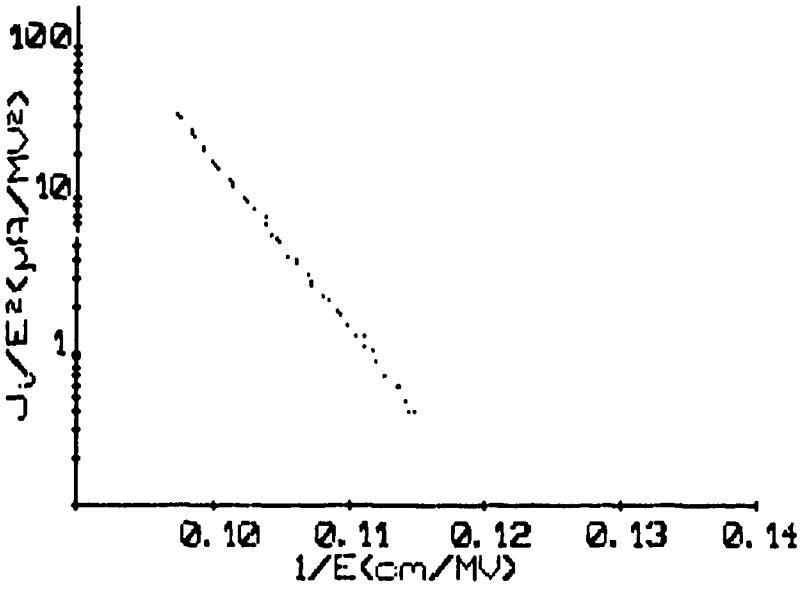

Figure 17. Typical Fowler-Nordheim plot generated by F4I test system for an MOS capacitor sample.

current is measured and, if below the specified maximum value, recorded. The injection pulse amplitude and duration are measured upon each completion of the inner control loop, and a running total for the injected charge is calculated. Present status of the injection sequence (pulse voltage and duration, current, total charge) is displayed upon each completion of the outer control loop. When the total injected charge reaches the desired level, the injection sequence stops. The operator may then switch the sample to the C-V apparatus to observe the effect of the injection. Injection may be resumed under the same conditions by switching back to the F4I apparatus and specifying a new total charge level. In a typical case, injection of a sample to the equivalent of 1 krad(SiO_2) takes only seconds; injection to the equivalent of 1 Mrad(SiO_2) requires a few minutes. The apparatus can function unattended for the longer injection sequences.

6. TEST RESULTS USING PROTOTYPE SYSTEM

In this section, sample results are presented from injection test runs performed on several different types of MOS capacitor samples to illustrate the use of the prototype F4I system and to indicate some of the variety of effects that can be obtained through its use.

Figure 18 shows C-V curves for a dry-process 90-nm oxide sample with an aluminum gate electrode before and after injection to various electron fluences at 9 MV/cm. The background electric field between injection pulses was maintained at 4 MV/cm (gate positive). The numbers in parentheses after

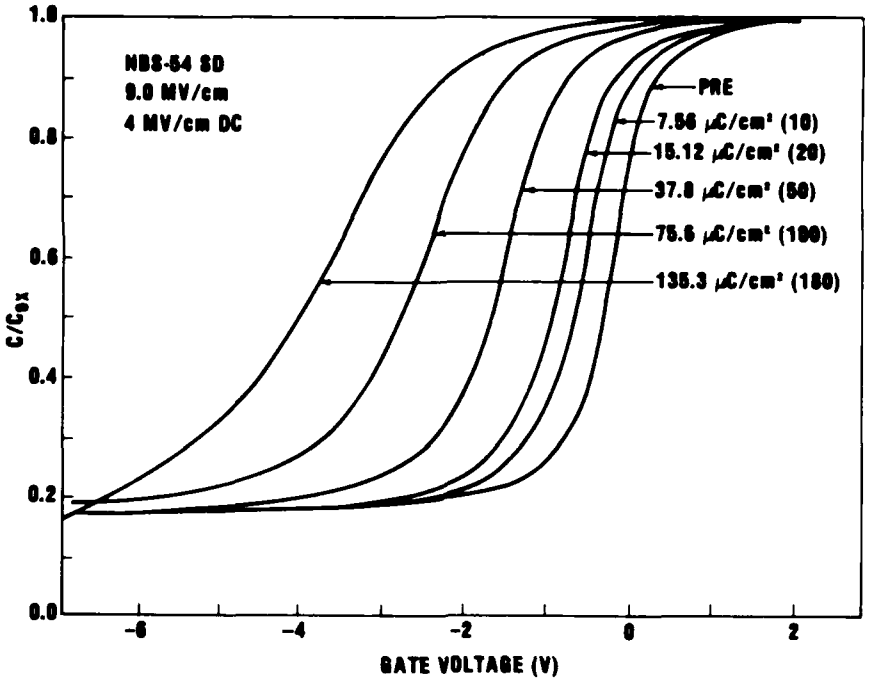

Figure 18. Capacitance-voltage characteristics for a radiation-soft 90-nm dry process oxide sample with Al gate before and after F4I injection to various electron fluences at 9 MV/cm. Numbers in parentheses are approximate equivalent ionizing radiation dose in krad(SiO_2).

each fluence correspond to the calculated equivalent ^{60}Co ionizing radiation dose in krad(SiO_2). Also indicated in the figure are the values of C/C_{ox} that correspond to the silicon surface potential being at midgap ($C = C_{mg}$) and flatband ($C = C_{fb}$). Flatband surface potential in n-type silicon corresponds approximately to the threshold voltage in an equivalent n-channel MOS transistor. At midgap surface potential, the interface states are generally thought to be uncharged; hence, midgap voltage shifts are attributed to oxide charge trapping alone. The difference between the midgap and flatband voltage shifts is a measure of the contribution of charge on interface states to the flatband voltage shift [17]. In the present case, the flatband shifts are consistently negative and fairly large, indicating that the ionizing radiation response of the equivalent MOS transistor would be dominated by trapping of the radiation-generated holes. The curves also show some evidence of interface-state build-up (increasing distortion) with injection fluence. However, the flatband and midgap shifts are almost the same, which indicates again that the interface states are not contributing significant (negative) charge to the flatband shift in comparison to the trapped hole component. This oxide has not undergone any special processing to reduce hole trapping (radiation hardening) and is typical of standard commercial MOS material (ca 1977). Based on the observed F4I shift, a device employing this oxide would probably fail under irradiation at a dose between 10 and 50 krad(SiO_2).

Figure 19 shows pre- and post-injection C-V curves for a 66-nm oxide with a polysilicon gate electrode. This oxide has undergone special processing to reduce hole trapping (radiation hardening). This sample was injected to much higher fluences (by about a factor of 20) than for the previous case. Note that the flatband voltage first undergoes a small negative shift (to 528 $\mu C/cm^2$) and then moves positive. Meanwhile, the midgap voltage moves rapidly negative and offscale. Other curves indicate that the midgap voltage shifts monotonically negative with injection fluence. The C-V curves show severe distortion with increasing injection. In this case, a moderate buildup of trapped holes (positive charge produces negative voltage shift) is being compensated by a substantial buildup of interface states (negative charge at flatband produces positive voltage shift at flatband). The result is that this oxide would show very little flatband voltage shift under irradiation, and the equivalent MOSFET would show very little threshold voltage shift. Unfortunately, the large buildup of interface states would probably substantially reduce the transconductance of the MOSFET.

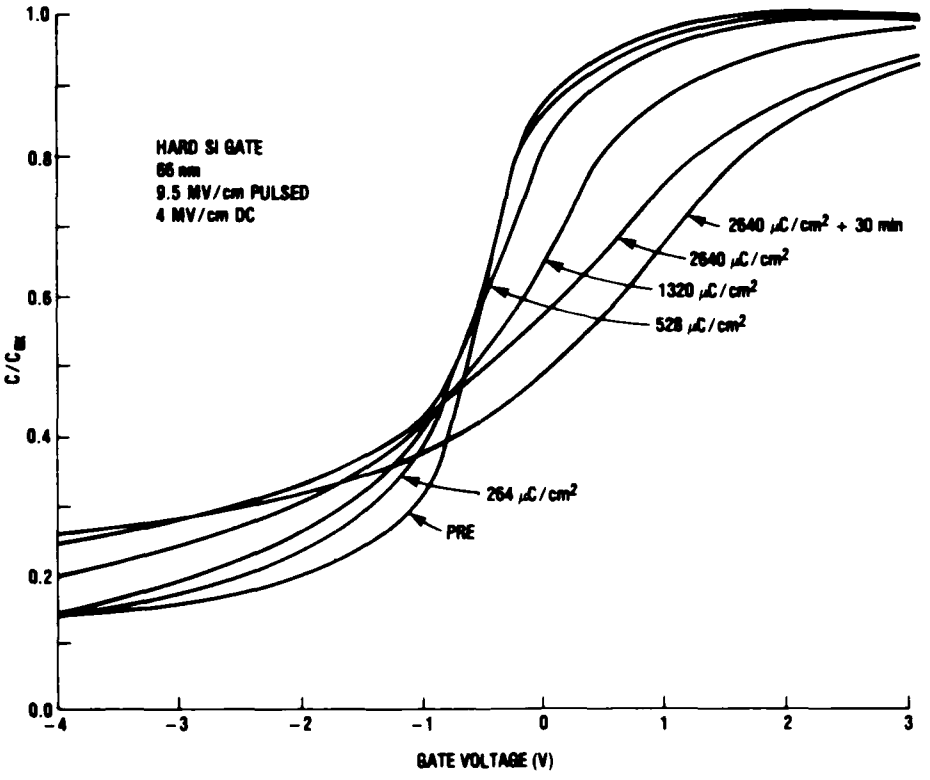

Figure 19. Capacitance-voltage characteristics for a radiation-hardened 66-nm oxide with a polysilicon gate before and after F4I injection at 9.5 MV/cm.

By virtue of the ability to vary the background (dc) bias on a sample independently of the injection pulse amplitude during an F4I test, the F4I test allows variation of the relative magnitudes of the hole trapping and interface-state buildup effects in an oxide. Figures 20 and 21 show C-V curves for radiation-hardened 80-nm oxide, polysilicon-gate MOS samples injected in identical sequences with 9-MV/cm pulses. The first sample (fig. 20) was injected with a positive 1-MV/cm background field; the second (fig. 21) was injected with a negative 1-MV/cm background. Both samples show small flatband voltage shifts to moderately high electron fluences (about 1 Mrad(SiO_2) equivalent). Both samples also show essentially identical negative midgap voltage shifts (with the exception of some offset at the lower fluences), indicating nearly equal hole trapping. However, substantial differences exist in the details of the flatband voltage shifts and in the amount of distortion that builds into the C-V curves at higher fluences. The 1-MV/cm dc bias case (fig. 20) shows more distortion as well as less negative flatband voltage shift at lower fluences and a "turnaround" (the flatband voltage starts to shift in the positive direction) above 315 $\mu C/cm^2$. These differences are largely attributable to a difference in the magnitudes of interface-state buildup in the two samples: the sample injected with positive background bias shows the greater interface-state buildup. This result is in accord with observations that interface-state buildup is enhanced in oxides irradiated under positive bias and is reduced under zero or negative bias [18].

The differences in the flatband voltage shifts between the two cases are also shown in figure 22, which is a plot of the shifts as a function of injected charge. (In this case, the injected charge scale ($\mu C/cm^2$) is roughly equivalent to ^{60}Co dose (krad(SiO_2).) The negative flatband shift is slightly greater for the sample under positive bias at fluences below about 50 $\mu C/cm^2$; at higher fluences, the negative shift is greater in the negative-bias sample. These results can be interpreted as indicating that hole trapping effects dominate at low fluences (positive bias encourages movement to the SiO_2/Si interface of those holes still in the oxide bulk after an injection pulse, as well as the buildup of interface states), and interface-state buildup dominates at higher fluences. Similar effects are commonly observed in MOS devices under irradiation. In particular, the "turnaround" shown in the figure is a typical feature of the radiation response of the threshold voltage of n-channel MOSFET's.

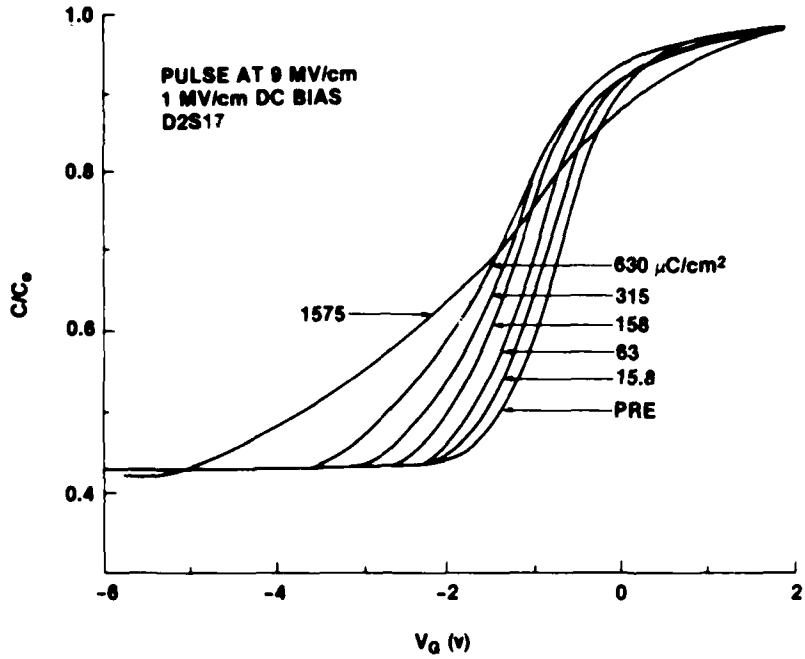

Figure 20. Capacitance-voltage characteristics for a radiation-hardened 80-nm oxide with a polysilicon gate before and after F4I injection at 9 MV/cm with a positive 1-MV/cm background field.

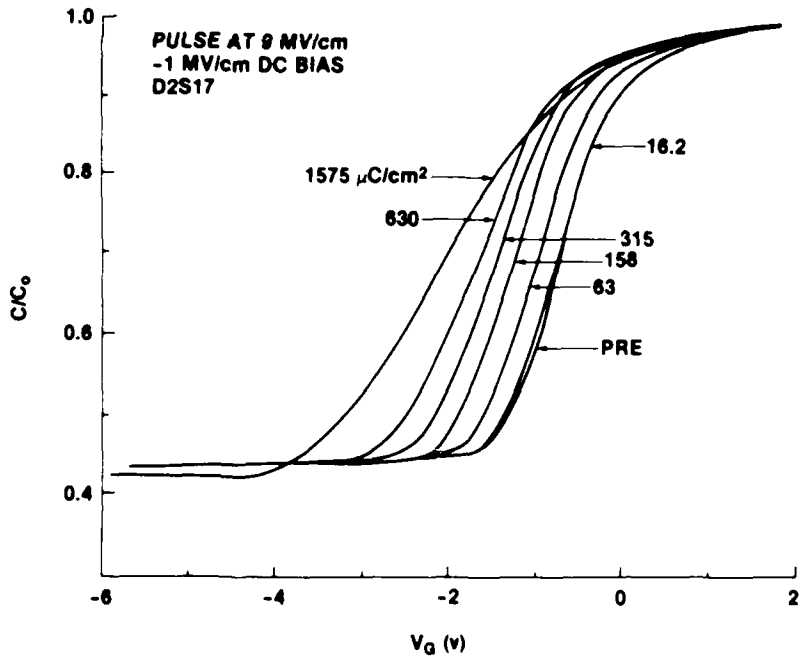

Figure 21. Capacitance-voltage characteristics for a radiation-hardened 80-nm oxide with a polysilicon gate before and after F4I injection at 9 MV/cm with a -1 MV/cm background field.

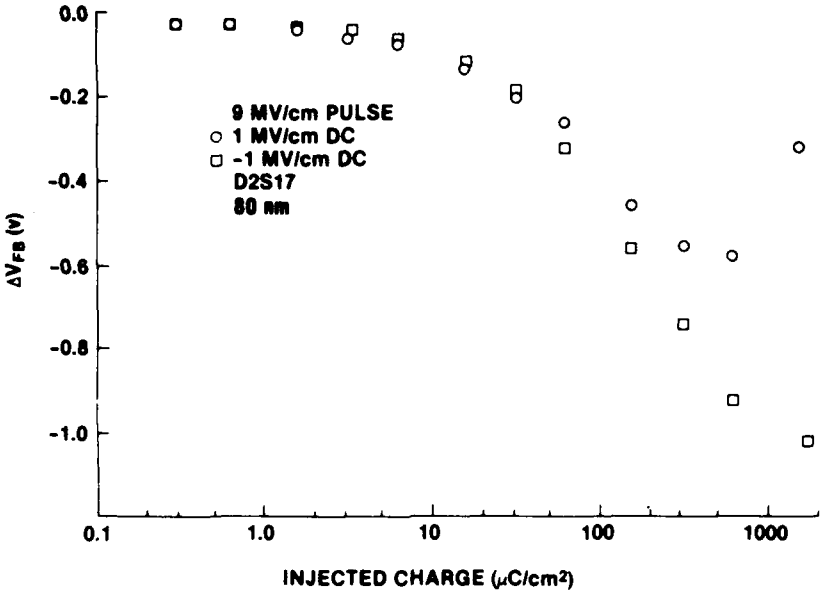

Figure 22. Flatband voltage shifts produced by F4I injection in radiation-hardened 80-nm oxide samples as a function of injected electron fluence at 9 MV/cm as extracted from data in figures 20 and 21. Circles are data points for sample injected with +1 MV/cm background field; squares are for sample injected with -1 MV/cm background field.

7. CONCLUSIONS

The theory, development, and operation of a prototype system for electrically measuring the radiation hardness of the most (total dose) radiation-sensitive regions of MOS integrated circuits--the silicon dioxide layers--have been described.

The technique employed in the system is the injection (by tunneling) of electrons into the oxide layer to be characterized by application of a pulsed high electric field across the oxide. The injected electrons then produce electron/hole pairs in the oxide by impact ionization; the holes thus generated then produce effects equivalent to that of exposure of the oxide to ionizing radiation. Thus the acronym, F4I, for the technique: field-induced injection and impact ionization.

The prototype F4I test system is microcomputer-based and provides for semiautomatic setup and execution of the injection test on MOS capacitor samples. Documentation of the more important test circuits, microcomputer operating programs, and operating procedures is contained in this report.

Dielectric (oxide) breakdown in the capacitor samples--a potentially serious problem for reliably executing the F4I test--was investigated, and sample configurations that avoid oxide damage were identified.

Examples were given of application of the F4I test to a variety of MOS samples with varying radiation hardness and processing history. Both hole trapping and interface-state buildup effects were produced in these samples by the test. Measurements of the radiation hardness of the samples as typified by the flatband voltage shifts correlated well with flatband voltage shift measurements performed in a conventional ^{60}Co ionizing radiation test source.

In addition to its possible use as a radiation hardness assurance test, the F4I test and system showed promise as a technique and tool for investigating the mechanisms for radiation damage in MOS structures [compare ref. 17]. In particular, the technique allows for greater separation and control of the processes of hole trapping and interface-state generation than is normally possible in conventional ionizing radiation experiments.

ACKNOWLEDGEMENT

The author wishes to acknowledge the contributions and support of James McGarrity, who originated the idea of using hole generation via impact ionization as a hardness assurance test and was involved in the initial effort to demonstrate the F4I technique.

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APPENDIX A.--SOFTWARE FOR PROTOTYPE MICROCOMPUTER-CONTROLLED F4I TEST SYSTEM

APPENDIX A

CONTENTS

This appendix contains listings of the BASIC language and Apple II 6502 microprocessor assembly language programs written to control the prototype F4I measurement system. Major features or functions of the BASIC main control program are outlined in table A-1 by statement number. The full BASIC program listing appears in listing A-1. Finally, the 6502 machine-language utility subroutines that enable the microcomputer to communicate with the F4I injection apparatus are listed in annotated assembler format in listing A-2.

TABLE A-1. F4I TEST.BAS
FUNCTIONAL OUTLINE

Statement No.	Function
1-6	Initialization.
7-13	Cold start: load ZAP.COM and relocate BASIC program.
90-100	Function definition; calibration constants.
102-105	Main menu.
300-310	Fowler-Nordheim plot menu.
402-410	Switch current range on overload.
500-600	Set current amplifier offset.
650-675	Save F-N plot to disk.
700-830	Run voltage ramp.
1000-1010	Set pulse duration offset.
1030-1050	Set current amplifier range.
1100-2000	Do injection sequence.
3000-3320	Get oxide thickness from F-N fit.
7000-7050	Save (V_I, I_I) array to disk.
7055-7120	Read (V_I, I_I) array from disk.
7200	Display injected charge.
7300	Read and display pulse amplitude, duration, and injected current.

APPENDIX A

TABLE A-1. F4I TEST.BAS
FUNCTIONAL OUTLINE (cont'd)

Statement No.	Function
8000-8300	Do F-N plot and least-squares fit with (V_I, I_I) array.
8400	Sound bell and display warning when current limit exceeded.
8500-8510	Output HV pulse, read and display amplitude, duration, and injected current.
8900-9025	Get voltage offset for HV pulse.
9040-9120	Input/calculate sample parameters.
9150-9160	Set maximum injection current limit.
9200-9280	Set current amplifier zero.
9300-9395	Get current amplifier calibration scale factors and save to disk.
9400-9420	Read current amplifier scale factors from disk.
9500	Time delay loop.
9600-9610	Display switch check reminder and wait for key.
9630-9660	Set current amplifier scale.
9700	Display "CHANGE?"; get key.

Listing A-1: F4I TEST.BAS

```
1  TEXT : PRINT "F4I TEST.BAS 1/14/83": GOTO 7
2 NP = 0:MI = 0:II = 0:CT = 0:CF = 0:KK = 0:DAP = 0:APD = 0:VC = 0:PA = 0:ZAP = 24693:ZMAX = 24726:PULSES = 24727:ZLOOP = 24736

3  DIM SC(5,4),X(100),Y(100),EI(100),JE2(100),CI(4)
4 KD = 5.45468E - 10:VC = 150 / 32768:KA = 218.45:ES = 3.40879E - 13
5 D$ =  CHR$ (4):OS = 2.74E - 4:IC = 1:K0 =  - 391:K1 = 4620:K2 = 139:K3 =  - 42:BHV = 49360:CI(1) = 20:CI(2) = 50:CI(3) = 200:
CI(4) = 500:JC = 4
6 INJ = 0: GOTO 15
7  INPUT "COLD (1) OR WARM (2) START? -> ";Z: IF Z <  > 1 THEN  GOTO 2
8  IF ( PEEK (24576) <  > 32 OR  PEEK (24577) <  > 12) THEN  PRINT  CHR$ (4);"BLOADZAP.COM3D A$6000,A$6000"
10  IF ( PEEK (16512) <  > 74 OR  PEEK (16513) <  > 56) THEN  PRINT  CHR$ (4);"BLOADF-N AXES.IMG,A$4000"
12  PRINT  CHR$ (4);"BRUNLOMEM A$330 L$A0": &  LOMEM: 24832
13  GOTO 2
15  POKE 10,76: POKE 11,0: POKE 12,96:MM =  USR ( - 1):MM =  USR (0)
90  DEF  FN LG(X) =  LOG (X) / 2.30258509: DEF  FN L10(X) =  FN LG(X) + 1
95  INPUT "GET CALIBRATION CONSTANTS FROM DISK?    (0=NO,1=YES) => ";Z: IF Z = 1 THEN  GOSUB 9400
100 BE = 12.30103:M =  - 103.362:MM =  USR (0)
102  TEXT : INPUT "VOLTAGE RAMP (1), SAMPLE INJECTION (2), PARAMETERS(3), F-N PLOT (4), ZERO CHECK (5), CALIBRATION (6) -> ";Z
103  ON Z GOSUB 700,1100,9050,300,500,9300
105 MM =  USR (0): GOTO 102
300  INPUT "FOWLER-NORDHEIM PLOT: PARAMETERS (1),   DATA FILE (2), PLOT (3), SAVE PLOT (4), FIT FOR L (5), RETURN (6) -> ";Z
305  ON Z GOSUB 9040,7055,8000,650,3000,102
310  GOTO 300
402  IF IC = 4 THEN  RETURN
410 IC = IC + 1: CALL  - 1054: PRINT "PLEASE SWITCH TO THE "CI(IC);" UA SCALE & HIT RETURN--": INPUT A$:CT = CT * SC(JC,IC - 1)
 / SC(JC,IC): GOSUB 9200: RETURN
500  PRINT "SET CURRENT AMP OFFSET (<CR> TO EXIT)"
505 V = 0: PRINT "V(PULSE) = 0": GOSUB 9700: IF A$ = "1" THEN  INPUT "NEW PULSE VOLTAGE -> ";V
510 IO = 0: GOSUB 1000: GOSUB 1030
590  GOSUB 8500:X =  PEEK ( - 16384): POKE  - 16368,0: IF X > 127 THEN  RETURN
600  GOTO 590
650 D$ = "": INPUT "PLOT FILE ID ?";NF$
660  PRINT D$;"BSAVEF-N PLOT.IMG ";NF$;", A8192,L8192": RETURN
670  PRINT "BSAVE F-N PLOT.IMG,A8192,L8192"
675  RETURN
700  GOSUB 1030
705  TEXT :TC = 0:T = 0:MM =  USR (KA * L * 4E6)
710  PRINT "STARTING V = ";VO: PRINT "MAX V = ";VM: PRINT "DV = ";DV: GOSUB 9700
715  IF A$ = "1" THEN  INPUT "STARTING VOLTAGE, MAX VOLTAGE, VOLTAGE INCREMENT -> ";VO,VM,DV
720  GOSUB 1000: GOSUB 9150
721  IF (VM - VO) / DV > 100 THEN  PRINT "DATA ARRAY WILL OVERFLOW": GOSUB 9700: IF A$ = "1" THEN  GOTO 720
724  GOSUB 8900: GOSUB 9220
730  FOR V = VO TO VM STEP DV:T = T + 1: IF T > 100 THEN T = T - 100
740  GOSUB 8500
765 X(T) = PA:Y(T) = I
785  IF I > IM THEN  GOSUB 8400: GOTO 800
790  IF  USR ( - 2) > 20000 THEN  GOSUB 402: GOSUB 8500:TD = 2000: GOSUB 9500
795 TC = TC + PD * I: NEXT
800 MM =  USR (0): PRINT "TOTAL CHARGE (UC) =";TC * 1E6
810  INPUT "RUN RAMP (1), SAVE DATA (2), RETURN (3) ?";Z: ON Z GOTO 820,830,2000
820  GOSUB 1030: GOTO 705
830  GOSUB 7000: GOTO 810
1000  PRINT "APPROX PULSE DURATION (US) = ";AD: GOSUB 9700: IF A$ = "1" THEN  INPUT "NEW PULSE DURATION (WITHIN 10 US) -> ";AD
1010 APD = (17.8795 *  INT (AD / 17.8795)) * 1E - 6 + 2E - 6: RETURN
1030  GOSUB 9630
```

Listing A-1: F4I TEST.BAS (cont'd)

```
1035  PRINT "CURRENT AMP RANGE = ";CI(IC): GOSUB 9700: IF A$ < > "1" THEN  RETURN
1037  INPUT "CURRENT AMP RANGE => ";CR
1040 IC = (CR = 20) + 2 * (CR = 50) + 3 * (CR = 200) + 4 * (CR = 500): IF IC < > 0 THEN  RETURN
1050  GOTO 1030
1100 TTC = 0
1105 TC = 0:CT = 0: GOSUB 9040:Z =  USR (KA * L * 4E6): GOSUB 1000: GOSUB 1030
1110  INPUT "PULSES/INNER LOOP?";NP: INPUT "PULSES/OUTER LOOP?";NK
1120  INPUT "INJECTION FIELD (MV/CM) -> ";EE:EE = EE * 1E6:VI = EE * L: PRINT "CALCULATED INJECTION VOLTAGE = ";.01 *  INT (100
 * V
1130 VI = EE * L: PRINT "INJECTION VOLTAGE (CALCULATED) = ";VI: GOSUB 9700: IF A$ = "1" THEN  INPUT "NEW INJECTION VOLTAGE => "
;VI
1131  GOSUB 8920: GOSUB 9220
1132 IP = A * 10 ^ BE * (VI / L) ^ 2 * 1E - 12 * 10 ^ (1E6 * M * L / VI): PRINT "PREDICTED I FOR ";.1 *  INT (10 * VI);" V = ";
.01 *  INT (100 * IP);" UA."
1134 QI = 1.56E - 6 *  EXP (1.8E8 * L / VI): PRINT "APPROX CHARGE NEEDED TO PRODUCE 1 KRAD  EQUIV DOSE = ";.001 *  INT (QI);" (
UC/CM2)."
1140  INPUT "CHARGE INCREMENT FOR THIS RUN (UC/CM2)?";FC: GOSUB 9150:TC = 0:CT = 0
1145 FC = FC * 1E - 6:INJ = 1: GOSUB 9230:INJ = 0:Z =  USR (0)
1155  GOSUB 9600: PRINT "STARTING INJECTION—"
1160 Z =  USR (218.45 * (VI + VOF))
1170 MI = IM / SC(JC,IC):CF = FC * A / (SC(JC,IC) * KD):DAP = APD / KD
1175  POKE ZMAX,120: IF MI / 256 < 120 THEN  POKE ZMAX,MI / 256
1176  PRINT "MI (STORED) = "; PEEK (ZMAX)
1190  POKE PULSES,NP: PRINT "INNER LOOP PULSES = "; PEEK (PULSES)
1200  FOR KK = 1 TO NK: CALL ZLOOP:II =  USR ( - 2) - IO: IF II > MI THEN  GOSUB 7300: GOTO 1300
1210 ZCNT =  PEEK (250):CT = CT + ( USR ( - 4) + DAP) * II * (NP - ZCNT): IF CT > CF THEN  GOTO 1350
1215  IF ZCNT > 0 THEN  PRINT ZCNT
1220  NEXT : GOSUB 7300
1245  GOSUB 7200: IF II + IO > 25000 THEN  GOSUB 7300: GOSUB 402: GOTO 1170
1250  GOTO 1190
1300  GOSUB 8400: GOSUB 1030: GOTO 1400
1350  PRINT "INJECTION COMPLETE"; CALL  - 1054: GOSUB 7200
1400 TTC = TTC + TC: PRINT "TOTAL INJECTED CHARGE (UC/CM2)          = ";.01 *  INT (1E8 * TTC)
1410  INPUT "CONTINUE INJECTION AT SAME FIELD (1),   AT NEW FIELD (2), OR RETURN (3) ?";Z: ON Z GOTO 1140,1105,2000
2000  RETURN
3000  PRINT "CALCULATE L FROM F-N DATA:":L1 = 1:LFIT = 1: GOSUB 9040: GOTO 8010
3100  PRINT "PLOTTED J/V2 NORMALIZED TO 100":JM =  - 1E + 20
3110  FOR J = 1 TO T: IF JE2(J) > JM THEN JM = JE2(J):EM = EI(J)
3120  NEXT :KY = 100 / JM:KX = 0.1 / EM
3130  FOR J = 1 TO T:EI(J) = KX * EI(J):JE2(J) = KY * JE2(J): NEXT : RETURN
3200  INPUT "ALTER PLOT (1), FIT LINE (2) OR RETURN (3) ?";Z: ON Z GOTO 3210,8260,2000
3210  GOSUB 9040: GOTO 8010
3300 LA =  SQR (2E + 12 / ((10 ^ BE) / KY)):LB =  - M *  LOG (10) * KX / 238
3310  PRINT "L FROM Y INTERCEPT = "; INT (1E9 * LA) / 10: PRINT "L FROM SLOPE = "; INT (1E9 * LB) / 10
3320  GOTO 3200
7000  GOSUB 9040: PRINT "DATA ARRAY LENGTH = ";T
7010  INPUT "F-N DATA FILE NAME ?";DF$
7015 D$ = ""
7020  PRINT D$;"OPEN ";DF$;",L32"
7025  PRINT D$;"WRITE ";DF$;",R0": PRINT T: PRINT C
7027  PRINT D$;"WRITE ";DF$;",R1": PRINT A: PRINT L
7030  FOR I = 1 TO T: PRINT D$;"WRITE ";DF$;",R";I + 1
7040  PRINT X(I): PRINT Y(I): NEXT
7050  PRINT D$;"CLOSE ";DF$: GOSUB 7065: RETURN
```

Listing A-1: F4I TEST.BAS (cont'd)

```
7055  PRINT D$,"CATALOG"
7060  PRINT "READ BACK DATA FILE:  INPUT FILE NAME?": INPUT DF$
7065 D$ =  CHR$ (4)
7070  PRINT D$;"OPEN ";DF$;",L32"
7080  PRINT D$;"READ ";DF$;",R0": INPUT T: INPUT C
7085  PRINT D$;"READ ";DF$;",R1": INPUT A: INPUT L
7090  FOR I = 1 TO T: PRINT D$;"READ ";DF$;",R";I + 1
7100  INPUT X(I): INPUT Y(I): NEXT
7110  PRINT D$;"CLOSE ";DF$: FOR I = 1 TO T: PRINT I;"  ";X(I),Y(I): NEXT
7115  PRINT "A(CM2)=";A,"L(ANG)="; INT (1E8 * L),"C(PF)="; INT (C)
7120  RETURN
7200 TC = FC * CT / CF: PRINT "INJECTED CHARGE (UC/CM2) = ";.01 *  INT (1E8 * TC): RETURN
7300 PA =  USR ( - 3) * VC: PRINT "V=";.1 *  INT (10 * PA);: HTAB 10: PRINT "T=";.1 *  INT (1E7 * ( USR ( - 4) * KD + APD));: H
TAB 20: PRINT "I=";1E - 5 *  INT (II * SC(JC,IC) * 1E11): RETURN
8000  GOSUB 9040:L1 = L:LFIT = 0
8010 SN = 0:SP = 0:SX = 0:SY = 0:XXS = 0:YYS = 0
8030  FOR J = 1 TO T:EI(J) = L1 / (X(J) * 1E - 6):JE2(J) = EI(J) ^ 2 * Y(J) / A / 1E - 6: NEXT
8035  HGR : HCOLOR= 3: POKE 60,0: POKE 61,64: POKE 62,0: POKE 63,96: POKE 66,0: POKE 67,32: CALL  - 468
8040  INPUT "STARTING INVERSE FIELD => ";SEI: INPUT "ENDING INVERSE FIELD => ";EEI
8050  IF LFIT THEN  GOSUB 3100
8060  FOR J = 1 TO T
8070  IF EI(J) > SEI OR EI(J) < EEI OR JE2(J) < .1 THEN  GOTO 8115
8080 XP = K0 + K1 * EI(J)
8090 YP = K2 + K3 *  FN L10(JE2(J))
8100  IF XP < 0 OR XP > 279 OR YP < 0 OR YP > 159 THEN  GOTO 8112
8110  HPLOT XP,YP
8112 SN = SN + 1:SP = EI(J) *  FN LG(JE2(J)) + SP:SX = EI(J) + SX:SY =  FN LG(JE2(J)) + SY:XXS = EI(J) ^ 2 + XXS
8115  NEXT
8117  IF LFIT THEN  GOTO 3200
8120  INPUT "ALTER PLOT (1), FIT LINE (2), OR RETURN (3) ?";Z: ON Z GOTO 8000,8260,2000
8260 M = (SN * SP - SX * SY) / (SN * XXS - SX ^ 2)
8270 BE = (SY * XXS - SX * SP) / (SN * XXS - SX ^ 2)
8275  IF LFIT THEN  GOTO 3300
8280  PRINT "A (UA/MV2) (C. 2E12) = ";10 ^ BE: PRINT "B (MV/CM) (C. -238) = ";M *  LOG (10)
8300  GOTO 8120
8400  CALL  - 1054: PRINT "*** CURRENT LIMIT EXCEEDED ***": RETURN
8500 Z =  USR (KA * (V + VOF)): CALL ZAP:PA =  USR ( - 3) * VC:I = ( USR ( - 2) - IO) * SC(JC,IC):PD =  USR ( - 4) * KD + APD
8510  PRINT "A=";.1 *  INT (10 * PA);: HTAB 10: PRINT "D=";.1 *  INT (1E7 * PD);: HTAB 20: PRINT "I=";.00001 *  INT (1E11 * I):
 RETURN
8900  PRINT "SET VOLTAGE OFFSET:"
8910  PRINT "VOLTAGE SET POINT = ";VI: GOSUB 9700: IF A$ = "1" THEN  INPUT "NEW SET POINT (V) => ";VI
8920  PRINT "DISCONNECT SAMPLE TO AVOID PULSING      DURING SETUP ROUTINE"
9000  GOSUB 9600:BZ =  USR (218.45 * VI):TD = 15000: GOSUB 9500
9020  CALL ZAP: FOR I = 1 TO 20: NEXT :PA =  USR ( - 3) * VC: P      "PULSE VI=";.1 *  INT (10 * VI),"VT=";.1 *  INT (10 * PA)
9025 VOF = VI - PA: PRINT "VOF = ";VOF:Z =  USR (0): RETURN
9030  GOTO 9010
9040  PRINT "SAMPLE PARAMETERS: L (A) = "; INT (1E8 * L);"  A (CM2) = "A;"  C (PF) = "; INT (C + .5)
9045  GOSUB 9700: IF A$ < > "1" THEN  RETURN
9050  INPUT "SAMPLE CAPACITANCE (PF) -> ";C: INPUT "GATE DIA (MILS) (0 IF NOT ROUND) -> ";D: IF D <  > 0 THEN A = 3.1415926 * (
D / 2 * 2.54E - 3) ^ 2: GOTO 9100
9060  INPUT "GATE LENGTH, WIDTH (MILS) (0'S IF NOT   RECTANGULAR) -> ";LL,WW:A = 6.4516E - 6 * LL * WW: IF A <  > 0 GOTO 9100
9100  PRINT "GATE AREA (CM2) = ";A:L = A * ES / (C * 1E - 12): PRINT "CALCULATED OXIDE THICKNESS (A) = ";L * 1E8
9110  GOSUB 9700: IF A$ = "1" THEN  INPUT "OXIDE THICKNESS (A) -> ";L:L = L * 1E - 8
9120  RETURN
9150  PRINT "CURRENT LIMIT (UA) = ";IM * 1E6: GOSUB 9700
```

Listing A-1: F4I TEST.BAS (cont'd)

```
9155  IF A$ = "1" THEN  INPUT "CURRENT LIMIT (UA) -> ";IM:IM = IM * 1E - 6
9160  RETURN
9200  IF IO = 0 THEN  RETURN
9210  GOTO 9250
9220  INPUT "USE IO=0 (0) OR READ IO (1)? ";Z: IF Z = 0 THEN IO = 0: RETURN
9230  PRINT "PULSE VOLTS FOR IO MEAS = ";VS: GOSUB 9700: IF A$ = "1" THEN  INPUT "NEW PULSE VOLTAGE => ";VS
9250  PRINT "VS = "; INT (VS * 100) / 100:Z =  USR (KA * (VS + VOF)):TD = 5000: GOSUB 9600: GOSUB 9500
9255  POKE ZMAX,255: POKE PULSES,1: IF INJ THEN  POKE PULSES,20
9256  PRINT "PULSES="; PEEK (PULSES)
9260 IO = 0: FOR I = 1 TO 20: CALL ZLOOP:IZ =  USR ( - 2):IO = IO + IZ: PRINT IZ,: FOR J = 1 TO 50: NEXT : NEXT
9270 IO = IO / 20: PRINT : PRINT "IO = ";1E - 5 *  INT (IO * SC(JC,IC) * 1E11)): IF IO < 16000 AND IO > 0 THEN  RETURN
9275  IF IO <  = 0 THEN  PRINT "IO OFFSCALE LOW: RESET": GOSUB 500: GOTO 9230
9280  PRINT "IO EXCESSIVE: RESET": GOSUB 500: GOTO 9230
9300  PRINT "CALIBRATE CURRENT AMPLIFIERS:"
9310  GOSUB 9630: GOSUB 1030: GOSUB 9220
9320  INPUT "CALIBRATOR CURRENT (UA) => ";IK
9325 IL = 0
9330  FOR I = 1 TO 20: CALL ZAP:TD = 20: GOSUB 9500:IL = IL +  USR ( - 2) - IO: NEXT
9340  IF IL <  = 0 THEN  PRINT "CURRENT OFFSCALE LOW": RETURN
9350 SC(JC,IC) = 2E - 5 * IK / IL: PRINT "SC(";JC",";IC;") = ";SC(JC,IC)
9360  INPUT "SAVE CALIBRATION CONSTANTS (YES=1,NO=0) => ";Z: IF Z <  > 1 THEN  RETURN
9365 D$ =  CHR$ (4): PRINT
9370  PRINT D$;"OPEN F4I CAL,L32"
9380  PRINT : FOR J = 1 TO 5: FOR I = 1 TO 4
9385  PRINT D$;"WRITE F4I CAL,R";(J - 1) * 5 + I
9390  PRINT SC(J,I): NEXT : NEXT
9395  PRINT D$;"CLOSE F4I CAL": RETURN
9400 D$ =  CHR$ (4): PRINT
9403  PRINT D$;"OPEN F4I CAL,L32"
9405  PRINT : FOR J = 1 TO 5: FOR I = 1 TO 4
9410  PRINT D$;"READ F4I CAL,R";(J - 1) * 5 + I
9415  INPUT SC(J,I): PRINT "SC(";J;",";I;") = ";SC(J,I): NEXT : NEXT
9420  PRINT D$;"CLOSE F4I CAL": RETURN
9500  FOR JJ = 1 TO TD: NEXT : RETURN
9600  PRINT "CHECK SWITCH POSITIONS & HIT RETURN          WHEN READY TO PROCEED": INPUT A$
9610  RETURN
9630  GOSUB 9660: GOSUB 9700: IF A$ = "1" THEN  GOSUB 9650
9640  RETURN
9650  PRINT "SET I/V AMP SCALE:": INPUT "0.1 -> 1000  (UA/V) => ";AA
9655 JC =  INT ( LOG (AA) /  LOG (10) + 2)
9660  PRINT "I/V SCALE = "; INT (10 * 10 ^ (JC - 2)) / 10;" UA/V": RETURN
9700  PRINT "(1 FOR CHANGE, <CR> FOR NO CHANGE)": INPUT A$: RETURN
10000  END
```

Listing A-2. Annotated ZAP.COM Assembly Language Utility Routines for F4I TEST.BAS

Entry routine (branch to desired utility):

```
6000-   20 0C E1   JSR   $E10C        USR (A)
6003-   A5 A0      LDA   $A0             A ≥ 0:  Set HV to A
6005-   C9 FF      CMP   #$FF            A = -1:  Initialize
6007-   D0 2A      BNE   $6033           A = -2:  Read I
6009-   A5 A1      LDA   $A1             A = -3:  Read HV pulse
600B-   C9 FF      CMP   #$FF            A = -4:  Read HV pulse duration
600D-   F0 0B      BEQ   $601A
600F-   C9 FE      CMP   #$FE
6011-   F0 43      BEQ   $6056
6013-   C9 FD      CMP   #$FD
6015-   F0 2E      BEQ   $6045
6017-   D0 70      BNE   $6089
```

Initialize interface cards (PIAs):

```
601A-   A9 BF      LDA   #$BE
601C-   8D 03 C4   STA   $C403
601F-   8D 03 C2   STA   $C203
6022-   29 00      AND   #$00
6024-   8D D1 C0   STA   $COD1
6027-   8D D2 C0   STA   $COD2
602A-   8D D5 C0   STA   $COD5
602D-   A9 01      LDA   #$01
602F-   8D D4 C0   STA   $COD4
6032-   60         RTS
```

Set HV pulse amplitude:

```
6033-   A5 A1      LDA   $A1
6035-   2A         ROL                   Store voltage set
6036-   8D D2 C0   STA   $COD2             in EW1100 board latches
6039-   A5 A0      LDA   $A0               (slot 5).
603B-   2A         ROL
603C-   8D D1 C0   STA   $COD1
603F-   60         RTS
```

Read HV pulse amplitude:

```
6045-   6E 00 C4   ROR   $C400
6048-   AD 01 C4   LDA   $C401           Shift values in $C400 (Hi Byte) and
604B-   6A         ROR                     $C401 (Lo Byte) (slot 4) into
604C-   A8         TAY                     accumulator and Y Reg
604D-   AD 00 C4   LDA   $C400
6050-   6A         ROR
6051-   29 7F      AND   #$7F
6053-   4C F2 E2   JMP   $E2F2           Convert to floating point and
                                           return to BASIC
```

Listing A-2. Annotated ZAP.COM Assembly Language Utility Routines for F4I TEST.BAS (cont'd)

```
Read injection current:

6056-   AD 01 C2   LDA   $C201        Loop until current
6059-   29 01      AND   #$01          value ready.
605B-   DO F9      BNE   $6056
605D-   6E 00 C2   ROR   $C200
6060-   AD 01 C2   LDA   $C201        Shift values in $C200 and $C201
6063-   6A         ROR                 (slot 2) into accumulator and Y Reg,
6064-   A8         TAY                 convert to floating point, and
6065-   AD 00 C2   LDA   $C200         return to BASIC.
6068-   6A         ROR
6069-   29 7F      AND   #$7F
606B-   4C F2 E2   JMP   $E2F2

606E-   A2 FF      LDX   #$FF          Time delay
6070-   CA         DEX                   loop.
6071-   DO FD      BNE   $6070
6073-   60         RTS

6074-   EA         NOP
6075-   8D D4 C0   STA   $C0D4         Output HV pulse.
6078-   60         RTS

Read HV pulse duration:

6079-   6E DO C0   ROR   $C0D0
607C-   6A         ROR
607D-   29 80      AND   #$80          Read shifted values (slot 5, EW1100
607F-   A8         TAY                   board), convert to floating point
6080-   AD DO C0   LDA   $C0D0           and return to BASIC.
6083-   6A         ROR
6084-   29 7F      AND   #$7F
6086-   4C F2 E2   JMP   $E2F2
6089-   C9 FC      CMP   #$FC
608B-   FO EC      BEQ   $6079          Check for correct
608D-   C9 FB      CMP   #$FB             entry point.
608F-   FO E2      BEQ   $6073
6091-   4C DO 00   JMP   $00D0
```

Listing A-2. Annotated ZAP.COM Assembly Language Utility Routines for F4I TEST.BAS (cont'd)

Fast injection: output HV pulse and check for excessive current

```
60A0-   AD 96 60   LDA   $6096        Set Max I.
60A3-   85 FB      STA   $FB
60A5-   AD 97 60   LDA   $6097        Store loop
60A8-   85 FA      STA   $FA            counter.
60AA-   8D D4 C0   STA   $C0D4        Output pulse.
60AD-   A9 01      LDA   #$01
60AF-   85 FC      STA   $FC          Time delay.
60B1-   20 6E 60   JSR   $606E
60B4-   C6 FC      DEC   $FC
60B6-   D0 F9      BNE   $60B1
60B8-   AD 01 C2   LDA   $C201        Loop until
60BB-   29 01      AND   #$01           current read
60BD-   D0 F9      BNE   $60B8          ready.
60BF-   AD 00 C2   LDA   $C200
60C2-   18         CLC                Read current.
60C3-   6A         ROR
60C4-   C5 FB      CMP   $FB          Compare with Max I;
60C6-   10 05      BPL   $60CD          quit if >Max I.
60C8-   C6 FA      DEC   $FA
60CA-   D0 DE      BNE   $60AA        Quit if done with loop;
60CC-   60         RTS                  else continue.
60CD-   C6 FA      DEC   $FA
60CF-   60         RTS
```

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